

DIGITAL DISPLAY OF CHARACTERISTIC
PARAMETERS OF ACTIVE RADIO FREQUENCY
TRANSMISSION SYSTEMS

Darl Paul Patrick

DUDLEY KNOX LIBRARY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA 93940

NAVAL POSTGRADUATE SCHOOL

Monterey, California



THESIS

DIGITAL DISPLAY OF CHARACTERISTIC
PARAMETERS OF ACTIVE RADIO FREQUENCY
TRANSMISSION SYSTEMS

by

Lt. Darl P. Patrick, USN

June 1974

Thesis Advisor:

R. W. Adler

Approved for public release; distribution unlimited.

T161732

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Digital Display of Characteristic Parameters of Active Radio Frequency Transmission Systems		5. TYPE OF REPORT & PERIOD COVERED Master's Thesis; June 1974
7. AUTHOR(s) Darl Paul Patrick		6. PERFORMING ORG. REPORT NUMBER
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Postgraduate School Monterey, California 93940		8. CONTRACT OR GRANT NUMBER(s)
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Postgraduate School Monterey, California 93940		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Naval Postgraduate School Monterey, California 93940		12. REPORT DATE June 1974
		13. NUMBER OF PAGES
		15. SECURITY CLASS. (of this report)
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Digital Display of Radio Frequency Parameters		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A concept for the digital display of radio-frequency parameters present on a transmission line terminated at an antenna is developed. Design criteria for the realization of this concept are established and discussed. The complete electronic and mechanical design, as well as fabrication of a prototype system analyzer is described in detail. Schematic diagrams of all electronic circuitry employed and photographs of prototype equipment are included. Preliminary performance test results are presented and discussed.		

DIGITAL DISPLAY OF CHARACTERISTIC PARAMETERS OF
ACTIVE RADIO FREQUENCY TRANSMISSION SYSTEMS

by

Darl Paul Patrick
Lieutenant, United States Navy
B.S.E.E., University of New Mexico, 1967

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL

June 1974

ABSTRACT

A concept for the digital display of radio-frequency parameters present on a transmission line terminated at an antenna is developed. Design criteria for the realization of this concept are established and discussed. The complete electronic and mechanical design, as well as fabrication of a prototype system analyzer is described in detail. Schematic diagrams of all electronic circuitry employed and photographs of prototype equipment are included. Preliminary performance test results are presented and discussed.

TABLE OF CONTENTS

I.	INTRODUCTION	11
II.	DIGITAL DISPLAY CONCEPT	14
	A. DESIGN CRITERIA	14
	B. THE SYSTEM	14
	C. STANDING WAVE RATIO (SWR) MEASUREMENT CIRCUIT DESIGN...	19
	D. LINEARIZING AND COMPUTING CIRCUITS	21
	E. SWR CONVERSION AND DISPLAY CIRCUITS	27
	F. FORWARD/REFLECTED POWER MEASUREMENT CIRCUIT	34
	G. ANALOG-TO-DIGITAL CONVERTER (A/D)	35
	H. TIMING AND CONTROL PULSES	35
	I. STANDING WAVE RATIO ALARM CIRCUIT	43
	J. ANTENNA SELECT CIRCUIT DESIGN	52
	K. FREQUENCY COUNTER DESIGN	56
	L. DIGITAL CLOCK CIRCUIT	59
	M. POWER SUPPLY DESIGN	60
III.	FABRICATION AND TESTING	64
	A. MECHANICAL FABRICATION	64
	B. LOGIC BOARD FABRICATION	64
	C. SUB-SYSTEM TESTING	65
	D. FREQUENCY COUNTER TESTING	66
	E. FORWARD/REFLECTED POWER BOARD TESTING	70
	F. SWR INDICATION BOARD TESTING	72
	G. SWR ALARM CIRCUIT TESTING :.....	76
	H. DIGITAL CLOCK TESTING	78
	I. SYSTEM TESTS AND RESULTS	78
	J. COMMENTS ON TEST DATA RESULTS	83

IV. CONCLUSIONS AND RECOMMENDATIONS	87
A. CONCLUSIONS	87
B. RECOMMENDATIONS	88
APPENDIX A Detailed Frequency Counter Operation	100
APPENDIX B	
1. Main Chassis Wiring Block Diagram	111
2. Power Supply Wiring Diagram	112
APPENDIX C Test Equipment Designed for Testing Digital Circuits.	114
APPENDIX D	
1. Photographs of prototype equipment	118
2. Printed circuit layouts for constructed boards	119/152

LIST OF ILLUSTRATIONS

Figure	Page
1. Radio Frequency "Power" Sensor	17
2. S.W.R. Meter Face	17
3. System Block Diagram	18
4. Sensor Output Voltage vs. Power	24
5. S.W.R. Calculator	25
6. S.W.R. Calculator Base Diagrams	26
7. S.W.R. Conversion and Display	31
8. S.W.R./Display Circuit Pulse Timing	32
9. S.W.R. Circuit Base Diagrams	33
10. Forward/Reflected Power Board	37
11. Analog-to-Digital Converter	38
12. Converter Timing Pulse Relationships	39
13. Timing Circuit	40
14. Timing Board Pulse Relationships	41
15. Converter/Timing Board Base Configurations	42
16. S.W.R. Alarm Board	49
17. Pulse Gate Relationships	50
18. Alarm Board Base Configurations	51
19. Antenna Select/Indication	54
20. Installation Diagram	55
21. Frequency Counter Block Diagram	58
22. Digital Clock Circuit	62
23. Power Supply Block Diagram	63
24. Frequency Counter Test Set Up	67

25. Forward/Reflected Power Calibration	71
26. S.W.R. Board Calibration	74
27. Linearizing Circuit Output vs. Sensor Voltage Output	75
28. System Test Set Up	79
29. Analog Multiplexer and Digital Converter	94
30. S.W.R. Digital Calculator	95
31. S.W.R. BCD Multiplex Input/Output Board	96
32. S.W.R. Program Board	97
33. Phase Angle Detector	98
34. Smith Chart	99
35. Frequency Counter Circuit	106
36. Timing Relationships	107
37. Overrange Detector Pulse Relationship	108
38. Frequency Counter Base Diagrams	109
39. Frequency Counter Power Supply	111
40. +5 volt, ± 15 volt Power Supply	112
41. Main Chassis Wiring Block Diagram	113
42. Digital Tester Block Diagram	116
43. Digital Test Set	117
44. Test System Configuration	119
45. System Analyzer Face Panel	120
46. System Analyzer Main Frame	121
47. System Analyzer, Top View	122
48. System Analyzer, Right Side View	123
49. System Analyzer, Left Side View	124
50. System Analyzer, Rear View	125
51. System Analyzer, Bottom View	126

52.	Power Supply, Face Panel	127
53.	Power Supply, Top View	128
54.	S.W.R. Calculator Board	129
55.	S.W.R. Calculator, Top View	130
56.	S.W.R. Calculator, Bottom View	131
57.	S.W.R. Conversion Board	132
58.	S.W.R. Conversion Board, Top View	133
59.	S.W.R. Conversion Board, Bottom View	134
60.	Display/Decoder Board	135
61.	Display/Decoder Board, Top View and Bottom View	136
62.	Forward/Reflected Power Board	137
63.	Forward/Reflected Power Board, Top View	138
64.	Forward/Reflected Power Board, Bottom View	139
65.	Timing Board	140
66.	Timing Board, Top View and Bottom View	141
67.	Digital Clock	142
68.	Digital Clock, Top View	143
69.	Digital Clock, Bottom View	144
70.	S.W.R. Alarm Board	145
71.	S.W.R. Alarm Board, Top View	146
72.	S.W.R. Alarm Board, Bottom View	147
73.	Frequency Counter	148
74.	Frequency Counter, Top View	149
75.	Frequency Counter, Bottom View	150
76.	Frequency Counter/Digital Clock Display Board	151
77.	Frequency Counter/Digital Clock Display Board, Top View and Bottom View	152

ACKNOWLEDGEMENTS

The author would like to express appreciation to NELC-Antenna Division for their interest and assistance in the development of this thesis. Appreciation is also expressed to Professor Adler and Professor Jauregui for their assistance and availability during the construction of the prototype model.

I. INTRODUCTION

Despite advances in transmitter configurations, antennas, and radio-frequency transmission lines, the measurement of radio-frequency power and standing wave ratios is still taken much as it was in the mid 1950's. The most commonly used device is the r.f. (radio-frequency) sensor, figure (1). The voltage of the forward traveling wave on a transmission line is sensed as is the voltage of the reverse or backward traveling wave. By proper scaling, these voltages are made proportional to the forward-power, P_f , and the reverse-power, P_r , on the transmission line. These voltages are then displayed on a meter which is calibrated in units of power, watts or kilowatts.

To obtain the standing wave ratio, SWR, the reverse power reading is divided by the forward power reading and the resultant of the division is square-rooted. The resultant number is added to one, and subtracted from one. The SWR is then obtained by dividing the sum by the difference as shown in equation (1).

$$SWR = \frac{1 + \sqrt{P_r/P_f}}{1 - \sqrt{P_r/P_f}} \quad (1)$$

Standard "measurement" of shipboard transmission lines and antennas is a little more primitive. A five-hundred volt megger is generally used to "test" the lines and antennas. If the megger shows no appreciable resistance to ground the transmission line and/or antenna is "good". There is no method of on-line testing to determine whether the impedances are correct, matched, deteriorating, or open.

Since a single meter is used to measure the forward as well as the reflected power of a given transmission line, the best accuracy which can be expected is $\pm 10\%$. A typical meter face, calibrated in units of power is shown to scale in figure (2). To obtain the SWR of the system requires reading the meter twice and performing the algebraic computations indicated in equation (1). This performance again introduces error since it is easier to divide whole numbers, the tendency is to round off the power levels read. A greater error arises from the unfamiliarity with equation (1) by most operators. When asked to compute the SWR of a system, given two power levels, most operators will divide the larger number by the smaller, add one to the result and subtract one from the result, then redive as shown in equation (2).

$$\text{"SWR"} \neq \frac{\frac{P_f}{P_r} + 1}{\frac{P_f}{P_r} - 1} \quad (2)$$

Utilizing equation (1) to compute the SWR, a value of 2.14 is realized for forward power of 173 watts and a reflected power of 23 watts. By using equation (2) a value of 1.33 is obtained for the SWR. The difference, 0.81, or 37.8% in this case indicates the degree of SWR error encountered. If equation (2) were used, and generally is, an operating system could easily be operated beyond design specifications.

Because of the computations required, most operators never compute the SWR. Instead a "maximum" P_r is devised, and provided the reverse power does not exceed this limit no concern is expressed for the systems

performance. In general this system works, but may allow the system to operate at the high end of design specifications with no corrective action being taken. This could result in failure of the transmission line and the antenna as well as any adjoining couplers.

What is actually required is a device which will measure the forward power and the reflected power on the transmission line and from these values compute the Standing Wave Ratio. The operator then has a tool which merely needs to be read to be used. Devices which accomplish these functions have been produced by Hewlett-Packard for the micro-wave frequencies, but there is as yet no comparable unit for the 0.2 to 30 MHz spectrum.

The purpose of this thesis then is to design and construct a device which will measure and display the forward power and the reflected power on a transmission line, and from these compute and display the SWR. Additionally, a frequency measuring device is included to give a numeric-digital readout of the frequency being measured, and an antenna select circuit allowing any one of N antennas to be tested or checked.

II. DIGITAL DISPLAY CONCEPT

A. DESIGN CRITERIA

To facilitate easy and accurate data display, a numeric Light Emitting Diode (LED) display was used. Three of the LED's are used for the forward power indication and are capable of indicating power levels from 10 to 999 watts. Three of the LED's are used for the reverse power indication, and are capable of indicating reverse powers from 1 to 99 watts. Three LED's are used to indicate the SWR. The two leading LED's are used to indicate the SWR. The two leading LED's have a dynamic range from 1.0 to 9.9. The trailing LED is held at a numeric 1. An additional indicating LED is used to indicate SWR conditions in excess of 9.9:1. Five LED's and an overrange light are used for the frequency counter, and an additional six LED's used for the clock indication.

The functions listed below were desirable in the composite function of the unit:

1. Six to nine digit accuracy for the frequency counter.
2. Programmable Standing Wave Ratio limits.
3. Visual and audible alarm for high SWR.
4. SWR overrange indication
5. Multiple antenna select capability.
6. Automatic transfer of transmitter to a dummy load if failure or high SWR occurs.
7. Internal test and calibration capability.

B. THE SYSTEM

Figure (3) illustrates the block diagram of the system. Figure (1) is a schematic of the "power-sensor" used. Both the forward and reflected

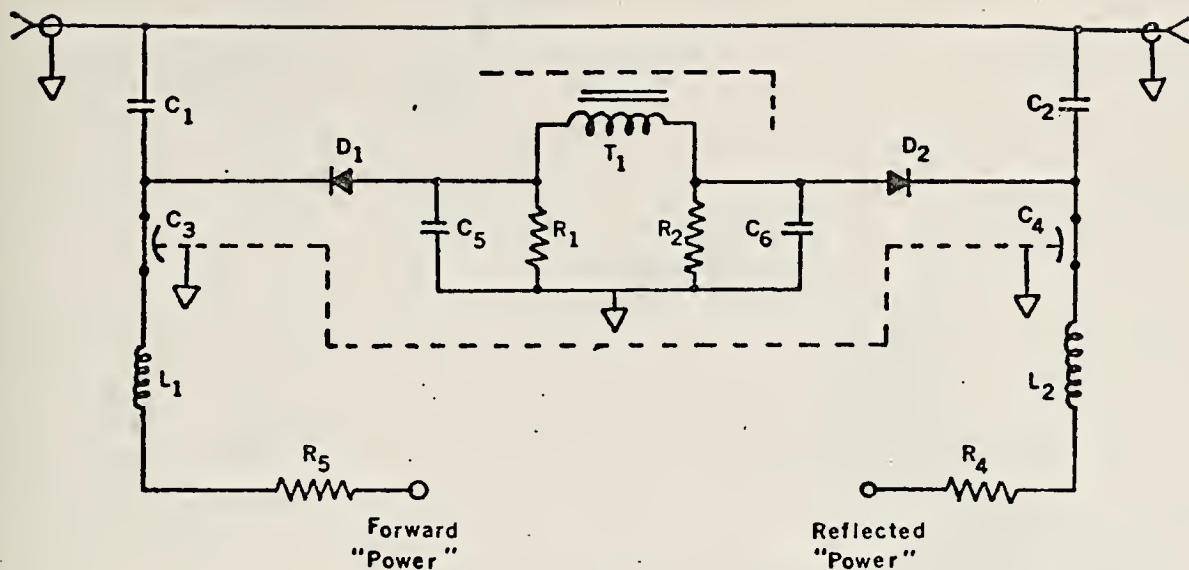
power is sensed and coupled to a linearizing circuit. The linearizing circuit conditions the input voltages so they are proportional to the input power levels. From the linearizing circuit the signals are split into two branches. One set of forward and reflected power signals are connected to an analog multiplexer, while the second set is connected to the standing wave ratio computing circuits. The signal pair delivered to the analog multiplexer is time shared and converted to a twelve bit, binary coded signal. The binary coded signal is demultiplexed and the resultant forward power binary coded signal, and the reflected power binary coded signal are decoded and displayed on their respective LED numeric indicators.

The second pair of signals sent to the SWR computing board is processed according to equation (1) in an analog format. The resultant signal is converted to a thirteen-bit binary code. The binary code is decoded and displayed on the respective LED's, with overrange indication.

The frequency on the transmission line is sampled and converted directly to a digital readout. The readout consisting of five LED's plus overflow, is capable of being switched between KHz (five digit readout) and MHz (five digit readout). The switching capability allows eight digit \pm one digit accuracy of frequency readout.

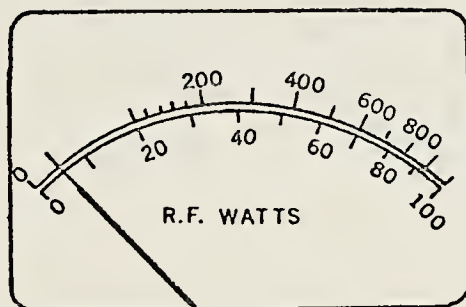
A SWR binary coded signal is coupled from the analog/digital converter to a set of digital comparators on the SWR alarm board. When the SWR signals exceed a manually preset signal level, the alarm board activates an audible as well as a visual alarm. Additionally the antenna selected is automatically dropped off the line and the transmitter terminated in a dummy load. When the alarm condition clears, the alarm circuitry remains in an alarm condition until reset manually by the operator.

Five antennas plus a dummy load are capable of being selected remotely from the control console. Each antenna has a visually labeled indicator which lights once the antenna relay has been selected and engaged. Failure of any of the antenna control circuitry results in an automatic switching of the transmitters to their respective dummy loads unless the circuitry is defeated by depressing the HI SWR alarm indicator light on the face panel of the console.



R.F. "Power" Sensor

Figure (1)



SWR Power Meter

Figure (2)

C. STANDING WAVE RATIO (SWR) MEASUREMENT CIRCUIT DESIGN

The Standing Wave Ratio is a number normally used to describe the operating characteristics of transmission systems. The term SWR is actually an indication of the "match" of a r.f. (radio frequency) system. If the transmitter is matched to the transmission line, and if the transmission line is matched to the antenna, the SWR would be 1:1. By the use of tuning circuits in the transmitter it is generally possible to match the transmitter circuitry to the transmission line used. It is not generally as easy to match the transmission line to an antenna. The amount of energy reflected by a discontinuity along any transmission line is measured in terms of the "reflection coefficient" (ρ). ρ is defined as:

$$\rho = \frac{E_i}{E_r} \quad (3)$$

Where E_i is the amplitude of the incident electric field, and E_r is the amplitude of the reflected electric field. The magnitude of E_r can vary from zero to a maximum equal to E_i . The reflection coefficient is always some value between zero and one. The Standing Wave Ratio is a measurement of the maximum voltage amplitude to the minimum voltage amplitude as shown in equation (4).

$$VSWR = \frac{1 + |\rho|}{1 - |\rho|} \quad (4)$$

By relating the amplitude of the incident and reflected electric field to power incident and reflected, equation (4) can be rewritten as:

$$VSWR = \frac{\sqrt{P_r} + \sqrt{P_i}}{\sqrt{P_i} - \sqrt{P_r}} \quad (5)$$

Since the power on the transmission line is equal to the voltage squared divided by the characteristic impedance of the line, $P=V^2/Z_c$, equation (5) can be written in the form of incident and reflected voltage.

$$VSWR = \frac{E_i + E_r}{E_i - E_r} \quad (6)$$

Since transmitters are normally rated in terms of power (watts or kilowatts), SWR meters are calibrated in watts and/or kilowatts. But either the measurement of power or voltage amplitudes will yield the same Standing Wave Ratio. When a meter movement is used to indicate the forward and reflected power no real problem is encountered. Since the meter movement is non-linear and the sensor is non-linear, it is a simple task to "mark" the face of the meter to correspond to known values of input power. Figure (2) shows a typical power meter used by the Navy. The problem arises in trying to read the meter when power levels are above mid-scale. As seen from figure (2) the spacing between marks decreases rapidly as the meter is calibrated across the meter face. At higher power levels the readout error becomes greater.

An additional problem arises when the readout is digitized. Digital systems are essentially linear, it cannot be "calibrated" to read values other than those which actually occur. Figure (4) show the sensor output voltage verses power on a transmission line. As shown by figure (4) curve A, the output voltage is not a linear function of input power.

For the first fifty watts of transmitted power the output voltage differential is 93 millivolts. While for the second fifty watts the change in output voltage is 47 millivolts. This change in the voltage differences changes the slope of the curve and accounts for the closer spacings of the power markings on the meter face. If a digital system were used to indicate the power on the transmission line, as a function of the sensed voltage, it would faithfully reproduce the non-linear curve giving erroneous readings. In order for a digital circuit to be utilized, curve A of figure (4) must be linearized and the slope shifted so that the output voltage differs from the input power by a constant scale factor as shown in figure (4) curve B.

Figure (5) is a schematic diagram of the Standing Wave Ratio calculating circuit. The design criteria is straight forward, for any two given input voltages which are proportional either linearly or non-linearly to power, the output must yield a value of SWR according to either equation (5) or (6).

From figure (4) it appears that it would be easier to use equation (5) and make the output voltage of the sensor proportional to power.

D. LINEARIZING AND COMPUTING CIRCUITS

Referring to figure (5), the linearizing circuit is composed of two 741 operational amplifiers (OP AMPS). A voltage fed into the "A" input is amplified and inverted by OP-AMP₁. The output of OP-AMP₁ is connected to the non-inverting input of OP-AMP₂ where it is amplified and fed back to the input of OP-AMP₁. The gain of the feed back OP-AMP₂ is controlled by a variable resistor, R₁₁. The feed back OP-AMP linearizes the input voltage curve so that a straight line is obtained at the output of OP-AMP₁. Resistor R₁₁, by adjusting the feed back loop gain of the feed back OP-AMP,

changes the slope of the output of OP-AMP₁. The linearized output of OP-AMP₁ is fed to OP-AMP₅ and to the input of the forward power measurement circuit, figure (7) input A, for processing and digital display. OP-AMP₅ is a times 10 multiplier, whose output is fed to a INTRONICS M530K operational amplifier connected as a square-root OP-AMP. The output of the M530K is $-\sqrt{10e_{in}}$. The linearized voltage was multiplied by a factor of 10 by OP-AMP₅, the output of the M530K is $-10\sqrt{e_{in}}$. The linearizing circuit and amplification of the "B" input is identical to input "A" up to this point. At point "C" a voltage equal to $-10\sqrt{P_f}$ is present. At point "D" there is a voltage equal to $-10\sqrt{P_r}$ present. These two voltages are summed at the inverting input of OP-AMP₉. The gain of OP-AMP₉ is set at 0.5, so the voltage out of the OP-AMP is equal to $5(\sqrt{P_f} + \sqrt{P_r})$. The analog voltage output of OP-AMP₉ is fed to OP-AMP₁₁ and to the inverting input of OP-AMP₁₀, where it is summed with the voltage at point "D". The resultant input voltage present at the inverting input of OP-AMP₁₀ is then equal to $5\sqrt{P_f} + 5\sqrt{P_r} - 10\sqrt{P_r}$. Summing the terms, and multiplying by a unity gain factor, the input of OP-AMP₁₀ is $-5(\sqrt{P_f} - \sqrt{P_r})$. The analog output of OP-AMP₁₀ is fed directly to the "Y" input of the M530K OP-AMP which is wired as a divider OP-AMP.

The second output of OP-AMP₉ is fed to a multiplying inverting operational amplifier, OP-AMP₁₁. The output of OP-AMP₁₁ is $-0.5(\sqrt{P_f} + \sqrt{P_r})$ and is fed to the "Z" input of the M530K divider OP-AMP.

The analog output of the M530K divider OP-AMP is $10(Z/Y)$. For the analog signals developed, the output equal to:

$$V_{out} = 10 \frac{-0.5(\sqrt{P_f} + \sqrt{P_r})}{-5(\sqrt{P_f} - \sqrt{P_r})} \quad (7)$$

The output voltage of the dividing OP-AMP is made equal to the SWR of the transmission system under measurement. There is one significant problem associated with the described method of determining SWR. The dynamic range of the M530K is ± 10 volts. The computed SWR is always greater than one which further limits the useful range of the M530K to SWR's less than 10:1. The limit of 10:1 for the SWR is not as limiting as expected however. A SWR ratio of 10:1 indicates a system in which 66.67% of the forward power is being reflected back from the load to the generator. This represents an impedance mismatch of 5:1. By the time this condition occurs the system should have been shut down. Failure to do so will result in transmitter damage.

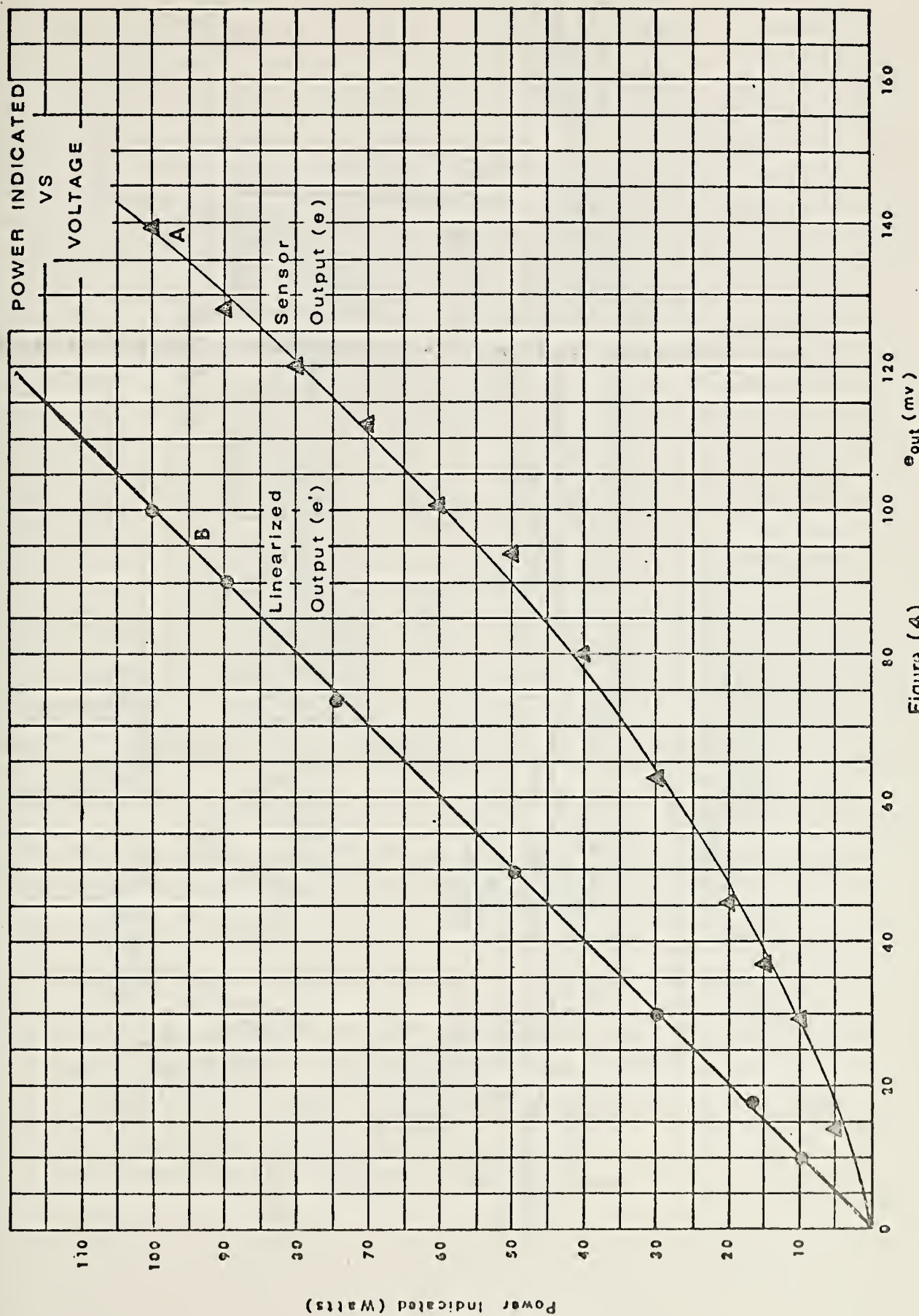
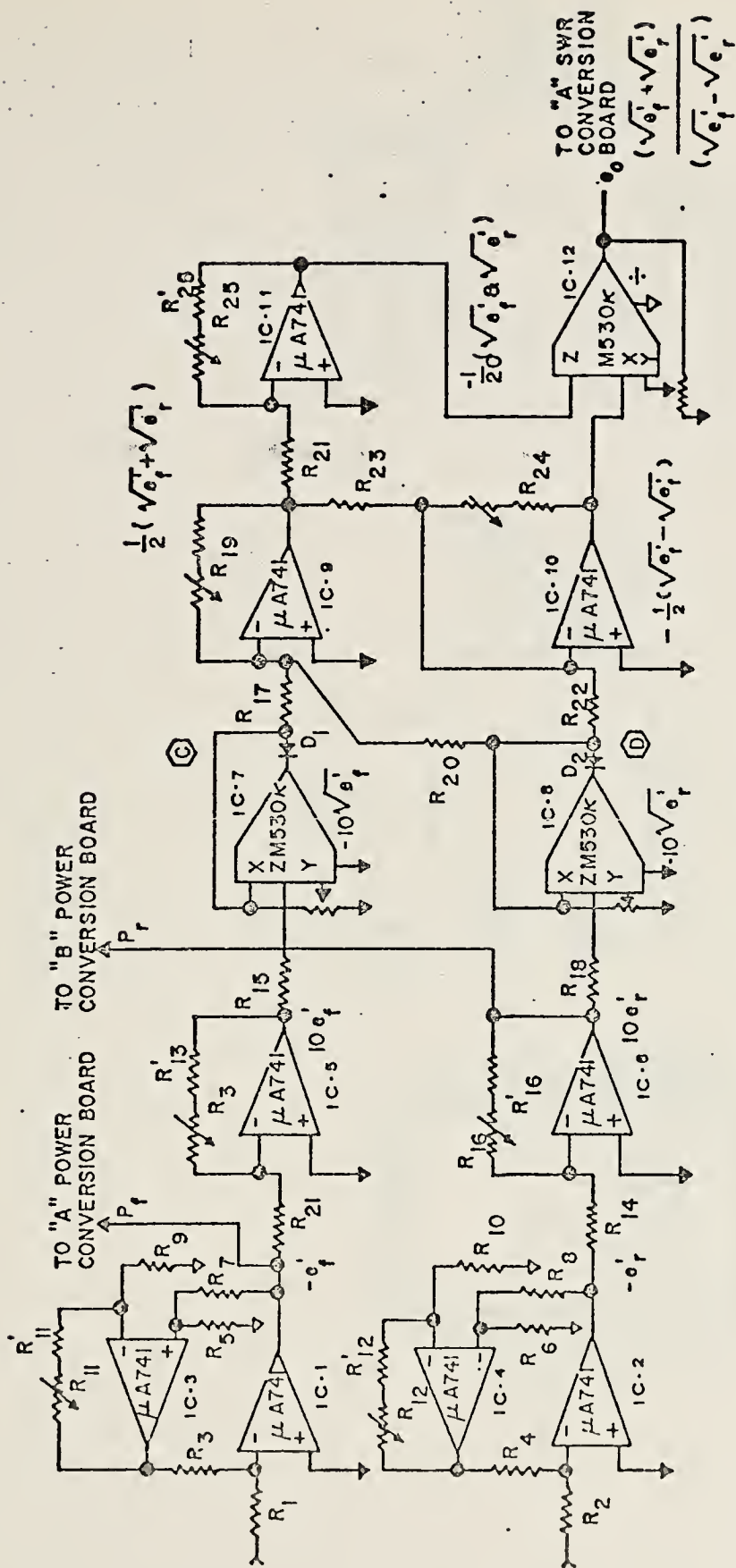


Figure (4)



SWR CALCULATOR
FIGURE (5)

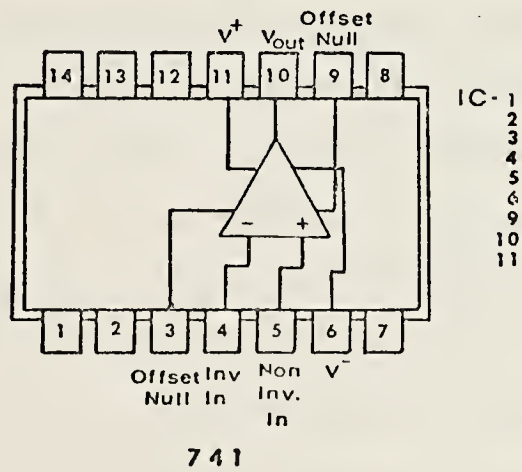
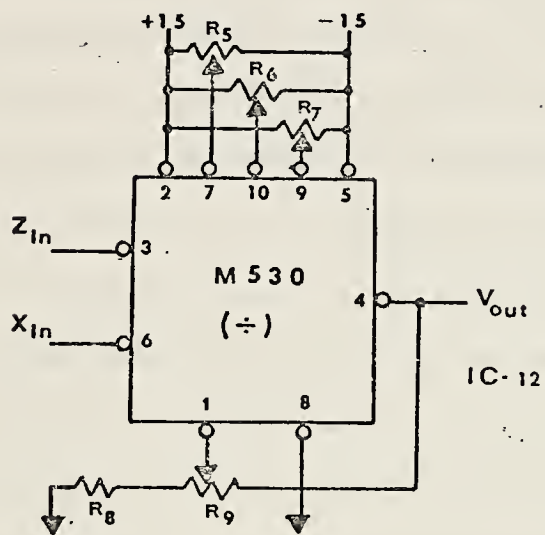
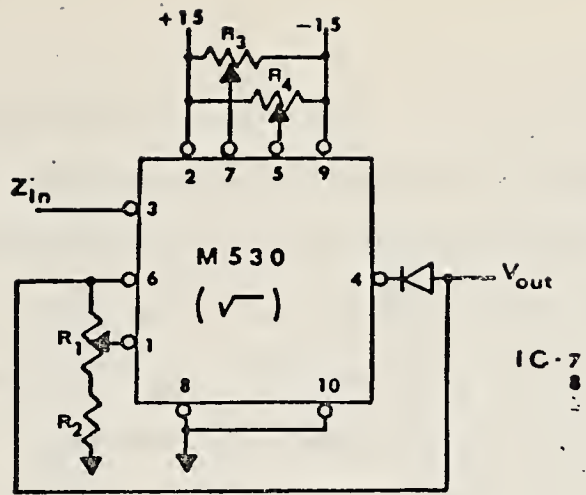


Figure (6)

E. SWR CONVERSION AND DISPLAY CIRCUITS

Figure (7) is a schematic diagram of the SWR conversion circuit and the latching, decoding, and display circuits. The SWR analog signal from the dividing OP-AMP is coupled to IC-1 on the SWR conversion board. IC-1 is a 741 operational amplifier with a 10:1 attenuator in the input. The 741 OP-AMP acts as a buffer between the attenuator and the analog-to-digital converter. The analog output voltage is 0.1 times the SWR analog signal input voltage. This scale reduction is necessary since the full scale range of the analog-to-digital converter is ± 2 volts. The output of IC-1 is fed directly to IC-8, a Datel 13-bit A/D converter. The analog information is converted to thirteen bits of binary coded data and fed to IC-2,3, and 4. IC-2,3, and 4 are digital latches which pass data when pins 4 and 13 are high, and hold any previous data when they are low (logic "0"). An end of conversion (EOC) pulse from IC-8 is fed to IC-6 and 7, one-shot monostable multivibrators. IC-6 is toggled by a negative going transistion (logic "1" to "0") with an output pulse duration of 10 microseconds (logic "1"). The 10 microsecond logic "1" pulse triggers IC-2,3, and 4 allowing the BCD data to pass through. When the Q output of IC-6 returns to logic "0" the BCD is latched, and held on pins 9,10,15, and 16 as usable data. The data is transferred to the inputs of IC-9 and 10. IC-7 is a positive-going triggered multivibrator, triggered by transistions from logic "0" to logic "1" of the EOC signal. The Q output of IC-7, a 10 microsecond logic "1" pulse, is used to trigger IC-9 and 10 to pass the BCD information to decoders IC-12 and 13 where the BCD data is decoded and displayed on the numeric LED's.

Overrange indication is provided by the thirteenth bit of the analog-to-digital converter. For analog values less than or equal to 9.99 the thirteenth data bit is at logic "0". When 9.99 analog, or 1001, 1001, 1001 binary is exceeded the overrange bit goes to a logic "1" which is used to bias a transistor into saturation. The load of the saturated transistor is a gas-discharge light.

The nominal analog voltages being measured lie in the low millivolt range. Initial testing indicated that it was possible to indicate a signal condition when the antenna/transmission line were used in a receive only mode. To eliminate any possibility of reading false signals during a system-down condition a DTL coincident gate was employed. An enabling signal (logic "1") is supplied by a relay which is activated by the transmitters antenna change-over relay. During transmit operation the logic "1" applied to the gate allows the triggering pulses to pass and the system operates as described. When the transmitter is idled, a logic "0" is applied to the gate which prevents the triggering pulses from passing. Since no new trigger pulses can pass, the last digital output is held on the numeric LEDs.

Figures (52), (53), and (54) show the constructed SWR computation board, SWR conversion board, and SWR decoder/display board.

An example of the SWR operation illustrates the various conversion operations. Assuming a sensor output of 140 millivolts from the forward power and 40 millivolts from the reflected power sensor. The forward power voltage is fed to IC-1 and the reflected power to IC-2 (figure 5). The forward power signal is linearized to a value of 100 millivolts (0.1 volts). From IC-1 the 0.1 volt signal is multiplied by a factor of 10 by IC-5 to a value of 1 volt. The 1 volt signal is

is square rooted according to $-\sqrt{10(1)}$ which yields an output of -3.16 volts at point "C". The reflected signal of 40 millivolts is linearized by IC-2 and IC-4 to give an output of 17.5 millivolts which is multiplied by 10 by IC-6. The output of IC-6, .175 volts, is square rooted according to $1\sqrt{10(.175)}$. The output of the second square rooter is -1.32 volts at point "D". The voltages at points "C" and "D" are summed at the summing node of IC-9 and amplified. The gain factor of IC-9 is 0.5 resulting in an output of +2.24 volts. The +2.24 volt output is fed to IC-11 as well as to the summing node of IC-10. At the summing node of IC-10 the output of IC-9 (+2.24 volts) is summed with the voltage at point "D" (-1.32 volts) and amplified by IC-10. IC-10 has a unity gain factor, and an output of -0.92 volts. The -0.92 volt analog signal is fed to the "Y" input of IC-12, an analog divider.

The output of IC-9 was also fed to IC-11. IC-11 is a 741 OP-AMP with a gain factor of 0.1. The output of IC-11, (-.224 volts) is fed to the "Z" input of IC-12, the analog divider. The analog divider acts on the "Y" and "Z" inputs according to $10(Z/Y)$. This operation results in an output of 2.4 volts. This value of voltage is equal to the SWR obtained from equation (5). By direct substitution into equation (5):

$$SWR = \frac{\sqrt{100} + \sqrt{40}}{\sqrt{100} - \sqrt{40}} = 2.44 \quad (8)$$

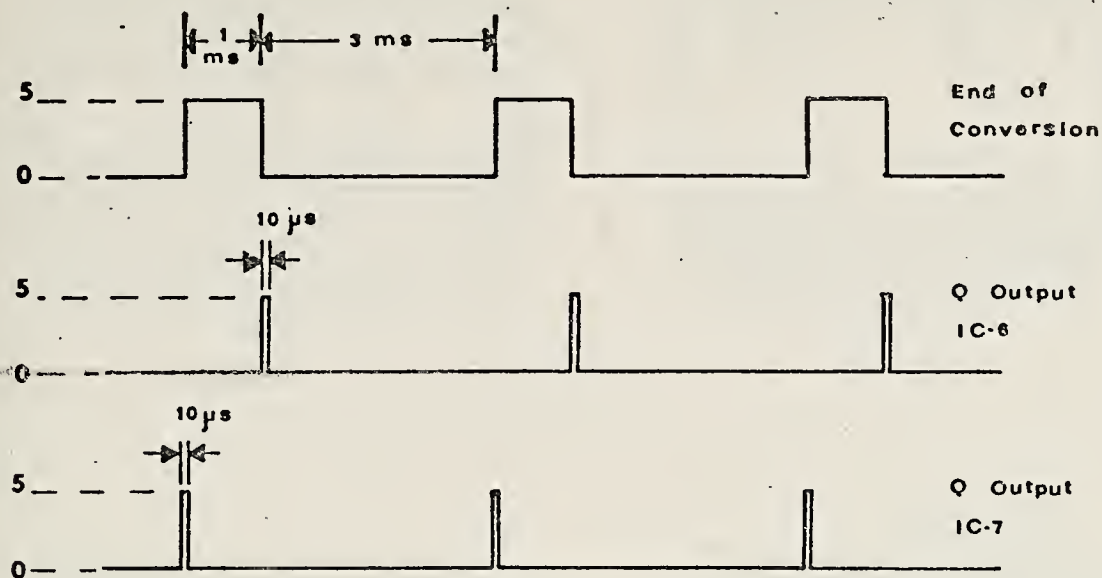
The computed value of SWR agrees with the electronically processed value.

The processing of the analog signals in the above example was based on an assumption that all of the components in the circuit operated ideally. In actual circuit operation there are many error factors

which can affect the output signal. The worst case assumptions will be briefly discussed. All of the 741 operational amplifiers must be corrected for off-set. The off-set is corrected by use of a 10 K-ohm pot. Provided an accurate D.C. voltmeter is available, the off-set can be set to 0 volts out for 0 volts in. The gain of the amplifiers is determined by the ratio of the feed back resistor and the input resistors. By making the feed back resistors variable, the correct ratio should be achieved. Due to availability of potenimeters, a 270 degree pot was used. These pots can generally, with care, be walked to within 5% of the desired value. This indicates a 5% error is probable in the output voltage. Assuming a 5% error per stage, the accumulated error at the input of the divider could be as great as 25% in the forward power leg, and 20% in the reflected power leg. The output voltage can then be written as:

$$10 \left(\frac{Z \pm .25Z}{Y \pm .20Y} \right) = \text{SWR} \quad (9)$$

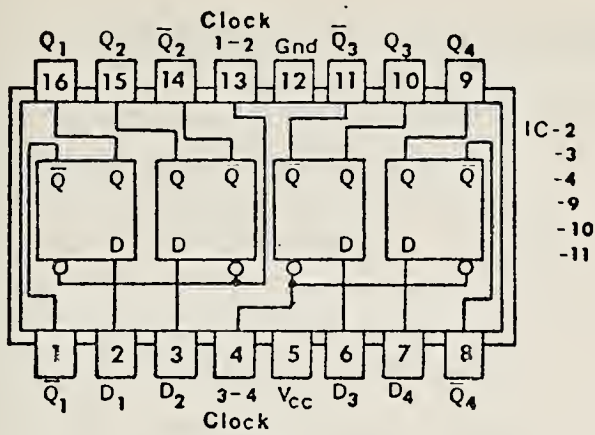
Solving equation (9) for the maximum and minimum possible error yields a maximum error of 1.56 and a minimum error of 0.625. The calculations ignore the possibility of cumulative errors in each leg cancelling. It is probable that the error will be less than calculated. The fact that an error exists is not as important as determining what the error is. The error present should be constant over the circuits operating range and a follow-on operational amplifier with a variable gain should be able to reduce the computed SWR to within 2.5% of calculated values.



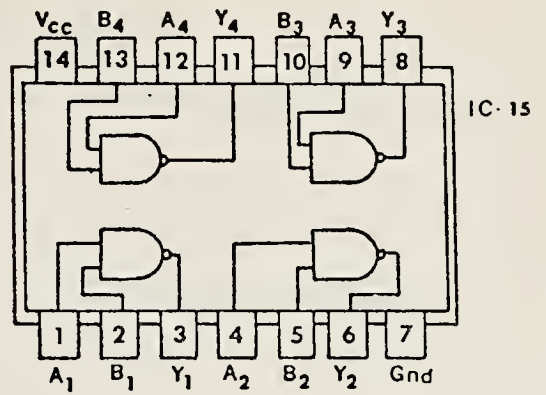
IC-6 is toggled by the negative going edge of the E.O.C. pulse. Data is transferred from the A/D converter to the holding latches IC-2,3, and 4 when Q_{out} of IC-6 is high. IC-7 is toggled by the positive going transistion of the E.O.C. pulse. Data is transferred from the holding latches to the display when the output of IC-7 is high (logic "1").

SWR/Display Circuit Pulse Timing Relationship

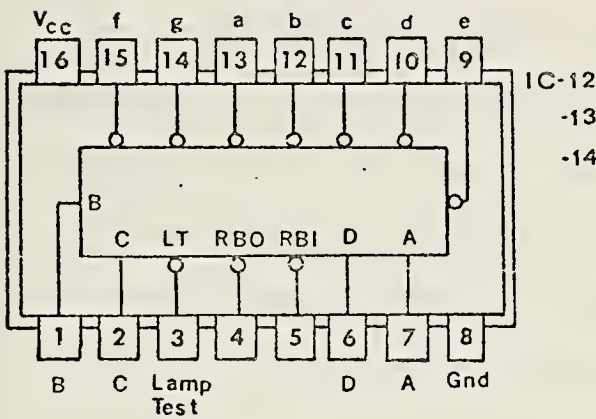
Figure (8)



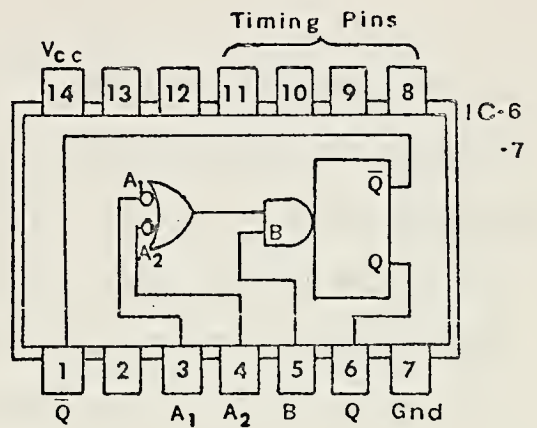
7475



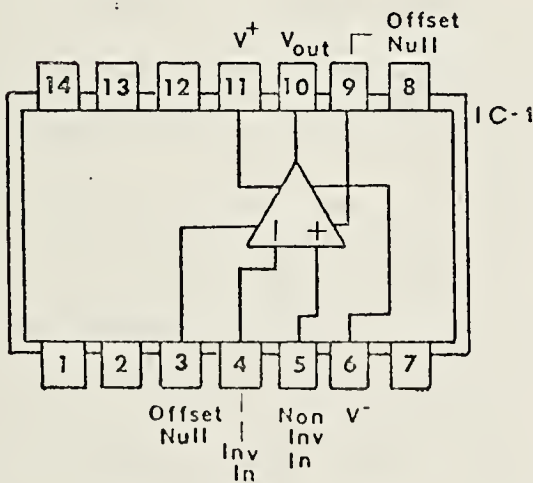
7400



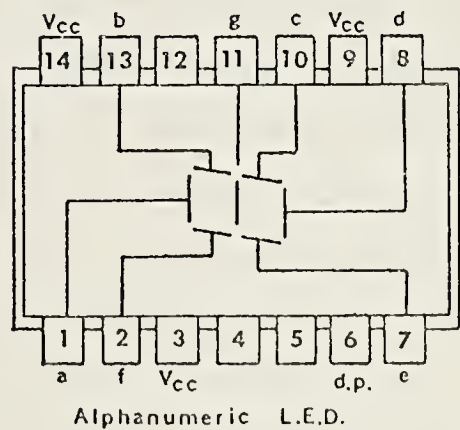
7447



74121



741



Alphanumeric L.E.D.

Figure (9)

F. FORWARD/REFLECTED POWER MEASUREMENT CIRCUIT

Figure (10) is a schematic diagram of the power measuring circuit.

Design specifications are:

- | | | |
|----|-------------------------------|---------------------------|
| a. | Counting Range | 0 to 999 watts forward |
| | | 0 to 99.9 watts reflected |
| b. | Accuracy | ± 1 digit |
| c. | Analog Multiplex input | |
| d. | Digital Demultiplexing output | |
| e. | Information update | 1/sec. |

Two linearized analog signals from the SWR circuit board which are proportional to the forward and reflected power, are multiplexed and fed to an A/D converter. The thirteen bit BCD coded output of the A/D converter is "latched" and held during the next count cycle. During each count cycle the information held in the latches is transferred to either the forward power or the reverse power storage latches. Each set of information is then transferred to the respective decoders and displayed on the numeric LEDs.

Referring to figure (10), the linearized analog voltages for forward power and reflected power are applied to inputs "A" and "B". Capacitors C_1 and C_2 remove any transients on the signal. Resistors R_1 and R_2 are scaling resistors used to adjust the linearized inputs for proper values. The scaled voltages are fed to IC-1 and IC-25, single throw, single pole DTL-compatible relays. IC-1 and 25 are alternately energized by the Q and \bar{Q} outputs of flip-flop IC-12. Information is transferred from IC-6,7,8,9,10, and 11 when a logic "1" is applied to pins 4 and 13, and held when they are held at logic "0". IC-6,7, and 8 are controlled by the Q output of IC-12 and IC-9,10, and 11 are controlled by the \bar{Q} output

of IC-12. When the Q output of IC-12 is at logic "1" IC-1 is energized, connecting the forward voltage analog signal to the A/D converter. The Q output simultaneously "opens" the gates (IC-6,7, and 8), passing the converted data from IC-3,4, and 5 to the holding latches IC-13,14, and 15. A timing pulse from the main timing board applies a logic "1" to IC-13,14, and 15 during the transfer of the reflected power signal to their respective latches. From the holding latches the information is decoded by IC-19,20, and 21 and displayed on the numeric LEDs.

G. ANALOG-TO-DIGITAL CONVERTER (A/D)

The analog-to-digital converter is constructed around the Data1 ADC-12E dual slope converter, figure (11). At the end of each conversion cycle a logic "1" to logic "0" transition occurs which triggers IC-2, a one shot multivibrator. The output of IC-2 is a 10 microsecond pulse (logic "1" out). The logic "1" output of IC-2 opens the gates of IC-3,4, and 5 allowing the converted signals to pass through the gates. The output of the gates is then available for routing through IC-6,7 and 8. The same sequence occurs for the reflected power when \bar{Q} of IC-12 goes to logic "1", except that IC-25 is energized and routing occurs through IC-9,10, and 11. Figure (12) shows the timing pulses for the A/D converter, bistable multivibrators, and IC-3,4, and 5.

H. TIMING AND CONTROL PULSES

The end-of-conversion pulse from the A/D converter is fed to an external timing board, figure (13), where it is fed to a flip-flop IC-26. IC-26 shapes the end-of-conversion (EOC) pulses to ensure sharp leading and trailing edges. The Q output of IC-26 is connected to pin 1 of IC-27, a divided -by-10 circuit. The output of IC-28 is a series

of pulses whose pulse repetition rate is 2 pulses per second. The pulse series is fed to IC-29 and IC-12, J-K flip-flops. IC-12, as explained, controls the gates of the latches IC-6,7,8,9,10, and 11, as well as selecting either IC-1 or IC-25. IC-29 is a J-K flip-flop with each of the Q and \bar{Q} outputs connected to a one-shot multivibrator, IC-30 and 31. IC-30 is triggered by the negative going (logic "1" to "0") transition of IC-29. The output of IC-30 is routed to the gating control of IC-13, 14, and 15 to control data transfer. The \bar{Q} output of IC-29 is used to toggle IC-31, a one-shot multivibrator wired to toggle on positive transitions. The Q output of IC-31 is routed to IC-16,17, and 18 to control data transfer. The Q outputs of both IC-30 and 31 are 10 micro-second pulses.

Figure (14) shows the timing pulse relationships figures (55) and (56) show the constructed power measuring board and the timing board.

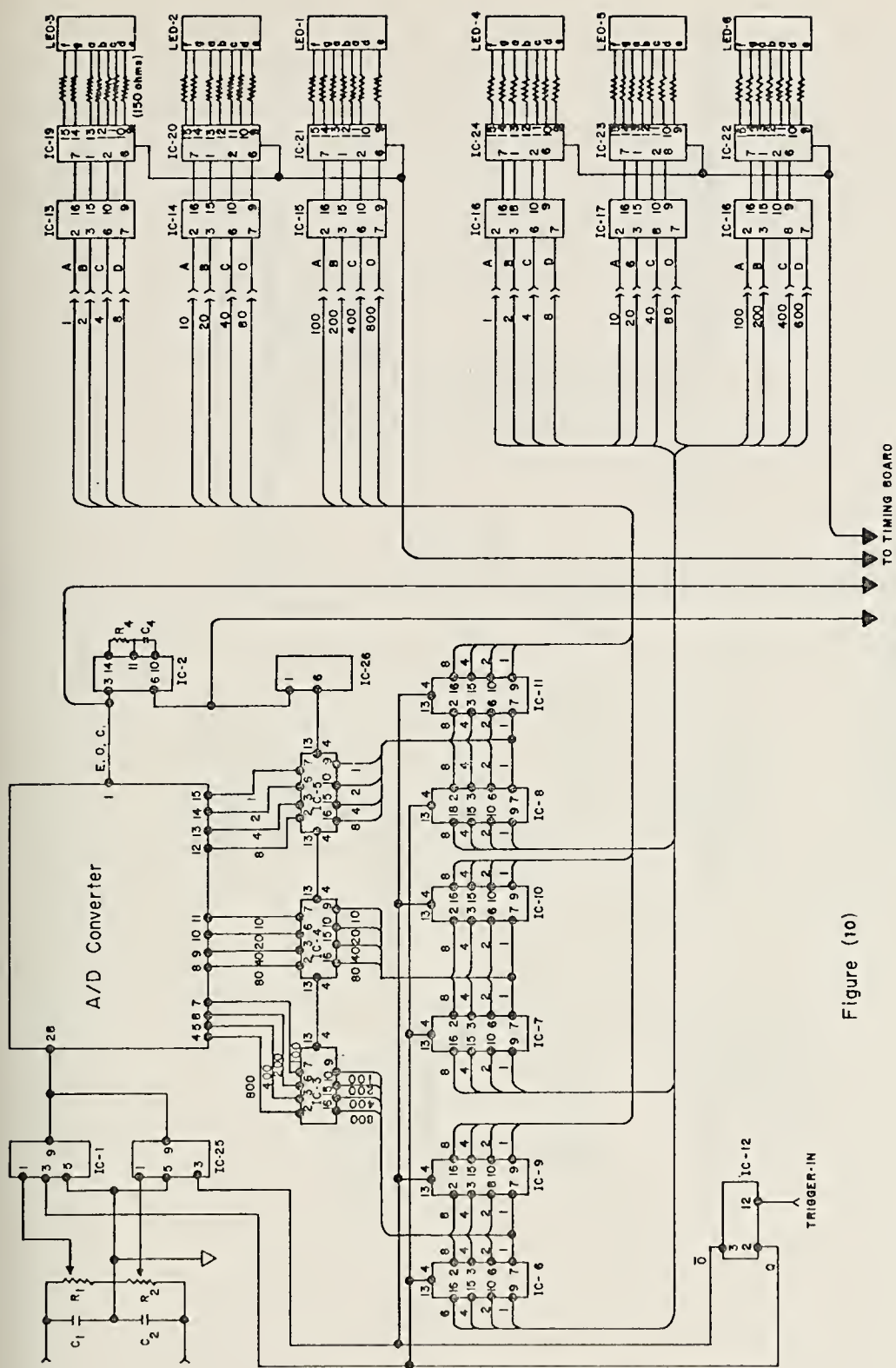
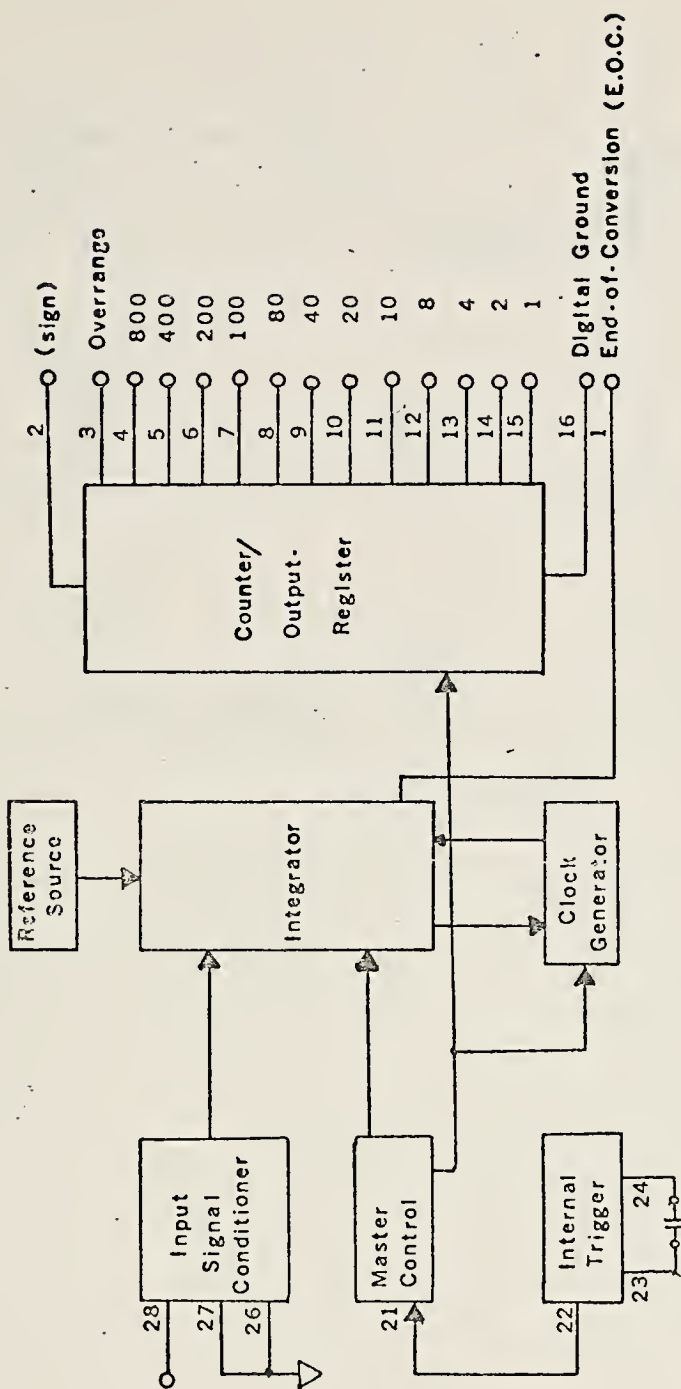


Figure (10)



Analog to Digital Converter

Figure (11)

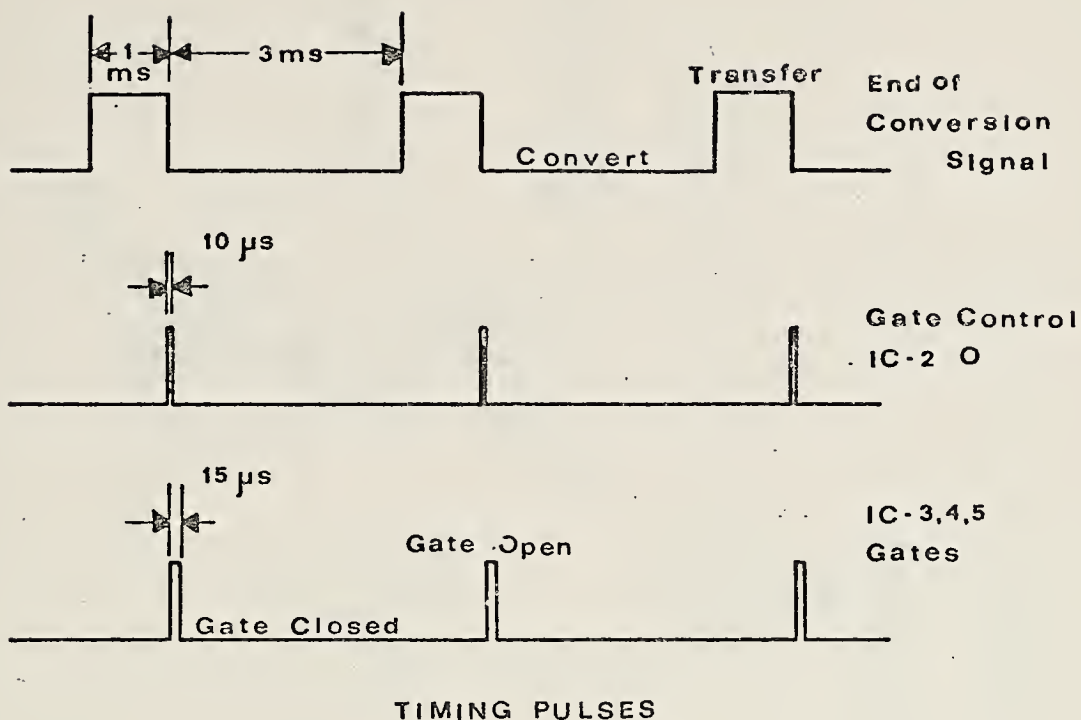


Figure (12)

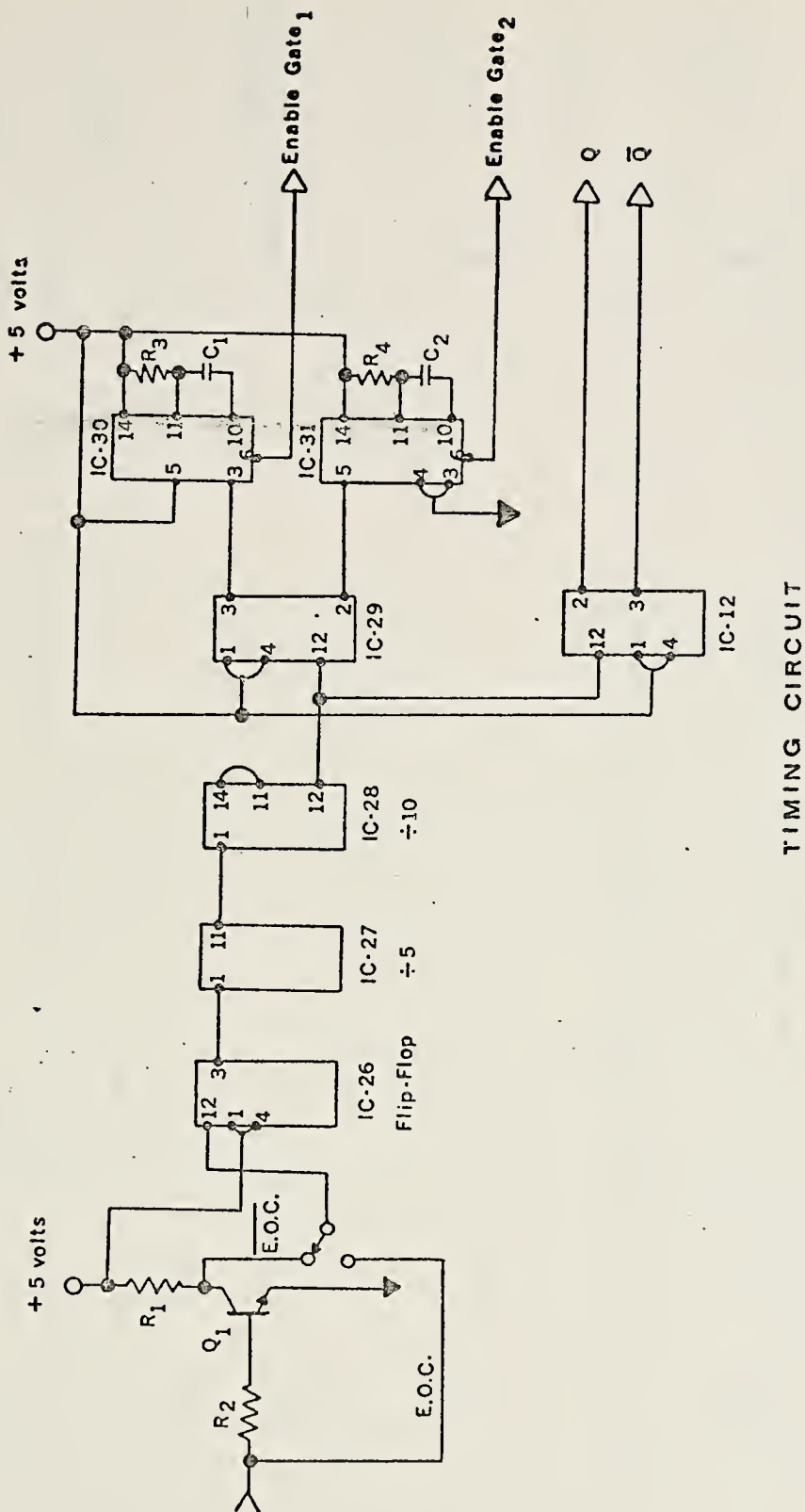


Figure (13)

Logic

E.O.C.

$\overline{\text{E.O.C.}}$

Q Fwd. Pwr.
Mux. Switch

\bar{Q} Refl. Power
Mux. Switch

Q₁ Fwd. Power
Data Transfer

Q₂ Refl. Power
Data Transfer

TIMING BOARD PULSE RELATIONSHIPS

Figure (14)

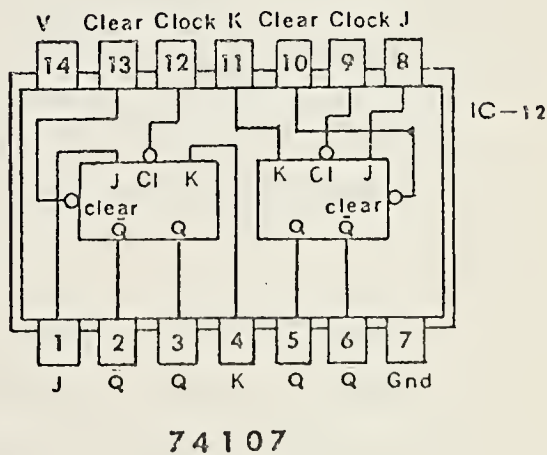
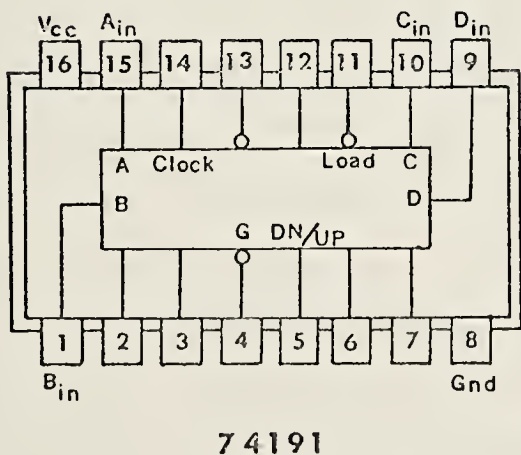
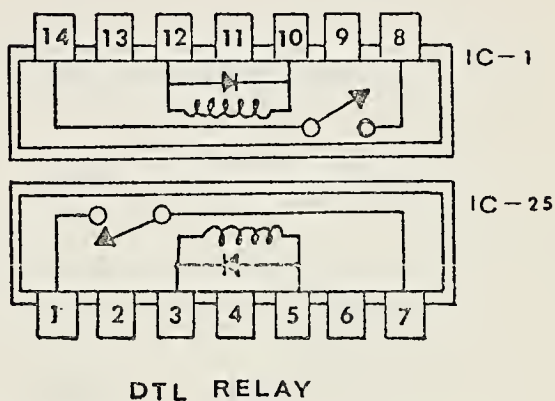
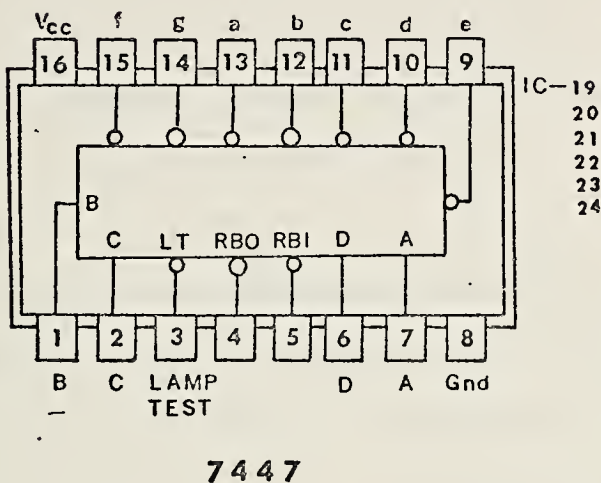
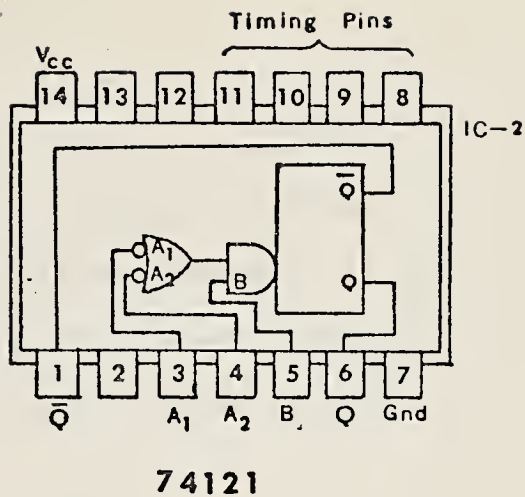
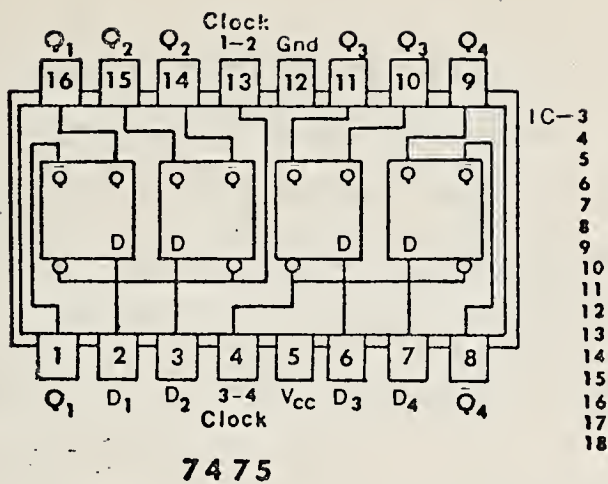


Figure (15)

I. STANDING WAVE RATIO ALARM CIRCUIT

The standing wave ratio, SWR, is used as an indicator of a radio-frequency, r.f., systems performance. It is possible for a high SWR condition to occur, and go unnoticed by the attending personnel. It is desirable therefore to design the alarm circuit for multiple function operation during a SWR alarm condition. The design criteria selected for the SWR alarm circuit is:

- a. Manual input of desired SWR threshold level.
- b. Audiable alarm when high SWR occurs.
- c. Visual alarm when high SWR occurs.
- d. Automatic transfer of connected transmitter to a dummy load.
- e. SWR lock and hold capability.
- f. Low error rate.

Refer to figure (16), for the following circuit description.

Switches S_{1-8} can be manually set for either a logic "1" or "0" state. Switches S_{1-4} constitute a binary word and is designated as the LSW (least significant word). Switches S_{5-8} constitute the MSW (most significant word). These switches provide a Binary Coded Decimal, BCD, input to IC-4 and 5, according to the code listed in table 1.

These binary word inputs (designated A-inputs), are compared in the binary comparators IC-4 and 5 against a second set of BCD inputs, (designated B-input). The B-inputs are taken from IC-2 and 3 from the SWR conversion board, figure (7).

If the MSW from the B-input exceeds the A-inputs, a SWR alarm condition exists. The output of IC-5, pin 6 changes to a logic "1" which is fed to IC-3. IC-3 acts as a buffer between IC-5 and the input of Q-4 and Q-5. When the input to IC-3 on pin 8 is a logic "1" (pin 9 at logic "0"), the output of IC-3 goes to logic "1" which is coupled to R_1 , C_3

DECIMAL	MSW	LSW
1.0	0001	0000
1.1	0001	0001
1.2	0001	0010
1.3	0001	0011
1.4	0001	0100
1.5	0001	0101
1.6	0001	0110
1.7	0001	0111
1.8	0001	1000
1.9	0001	1001
2.0	0010	0000
2.1	0010	0001
⋮	⋮	⋮
2.9	0010	1001
3.0	0011	0000
3.1	0011	0001
⋮	⋮	⋮
3.9	0011	1001
4.0	0100	0000
4.1	0100	0001
4.2	0100	0010
⋮	⋮	⋮
5.0	0101	0000
5.1	0101	0001
5.2	0101	0010
⋮	⋮	⋮
⋮	⋮	⋮
9.7	1001	0111
9.8	1001	1000
9.9	1001	1001

TABLE I

and the base of Q_4 . The logic "1" output of IC-3 charges C_3 through R_1 . If the logic "1" exists for a time period greater than five seconds, the voltage developed across C_3 due to its charge buildup is sufficient to turn Q_4 on, which in turn turns on Q_5 . Transistors $Q_{4,5}$ form a ground return for a DTL relay, IC-6. When a ground is supplied for IC-6, a short is placed across pins 1 and 7, energizing relay R_2 . When relay R_2 is energized the following occurs, 1) Contacts 2 and 3 close which provides a "lock-in" provision for R_2 . Even though the SWR may clear, returning pin 13 of IC-3 to a logic "0", discharging C_3 through D_1 and removing the short across pins 1 and 7 of IC-6, R_2 will remain in the energized condition. 2) Contacts 7 and 9 close providing +12 volts to a visual "HI SWR" alarm light on the front panel, and 3) contacts 5 and 6 close providing +5 volts to IC-1, Q_1 and Q_2 . IC-1 is a dual oscillator, set to oscillate at 1000 Hz and 1 Hz. Q_1 and Q_2 are buffer amplifiers with unity gain which isolate IC-1 from IC-2. The 1000 Hz output of IC-1 is coupled through buffer-amp Q_1 to pin 1 of IC-2. The 1 Hz output of IC-1 is coupled through buffer-amp Q_2 to pin 2 of IC-2. When both pins 1 and 2 of IC-2 are at logic "1", the output of IC-2, pin 6, is at a logic "1". The 1 Hz signal acts as a gate, allowing the 1000 Hz signal to pass through IC-2 for 1 second durations. The output of IC-2, pin 6, is coupled through R_8 to the base of Q_3 . Q_3 is a single stage audio amplifier which drives the loudspeaker with a frequency of 1000 Hz for 1 second periods. Figure (17) shows the gating relationships.

When the MSW-B-input exceeds the MSW-A-input a series of events occur which result in a HI-SWR alarm light on the face panel to be lit, a audible alarm to be energized and additionally the closing of contacts 7 and 9 of R_2 providing a +12 volts to switch the output of the transmitter from the manually selected antenna to a dummy load. Once the SWR

condition occurs and the system activates, it remains active until manually reset. The reset is accomplished by depressing the HI SWR alarm light which opens the SWR-switch removing power to R_2 which returns the circuits to their original condition.

If both the B-inputs to the MSW and the LSW are less than the A-inputs no SWR condition exists. It is possible for the B-inputs to the MSW to be equal to the A-inputs, and the B-inputs to the LSW to be greater than the A-inputs. This results in a SWR condition. For this condition the output of IC-5, pin 6, goes to a logic "1" and the output of IC-4, pin 7, goes to a logic "1". These signals are fed to pins 12 and 13 of IC-2. The output of IC-2, pin 8, goes to a logic "1" which is fed to pin 9 of IC-3, (pin 8 of IC-3 at logic "0"). With pin 8 at logic "0" and pin 9 at logic "1", the output of IC-3, pin 13, goes to logic "1" and the remaining circuits operate as previously explained.

The operation of the SWR alarm board can be further explained by the use of several examples. Assuming a desired SWR threshold point of 3.5:1, switches S_{1-8} are set as follows:

$S_{1,3,5,6}, \dots +5$ volt bus. (logic "1")

$S_{2,4,7,8}, \dots 0$ bus (logic "0")

The B-input of the MSW is 0011 (binary equivalent of decimal 3) and the LSW is 0101 (binary equivalent of decimal 5). As long as the SWR remains below 3.5:1, nothing happens. If, however, the SWR rises to a value greater than 3.5:1 the B-input of the LSW is compared against the A-input as is the B-input of the MSW. If the B-input of the LSW is greater than the A-input but the B-input of the MSW is less than the A-input of the MSW nothing results. If however, the B-input of the LSW

is greater than the A-input of the LSW and the B-input of the MSW is equal to or greater than the A-input of the MSW an output of logic "1" triggers the sequence of events which result in both a visual and an audible alarm, as well as tripping the antenna off the line and terminating the transmitter in a dummy load.

Table 2 shows the truth tables for IC-2,3,4, and 5. Figure (18) show the base configurations for the IC's used.

A	B	\bar{Y}
1	1	0
1	0	1
0	1	1
0	0	1

IC-2
Truth Table

A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

IC-3
Truth Table

Comparing Inputs				Outputs			
A3, B3	A2, B2	A1, B1	A0, B0		A B	A B	A=B
A3>B3	X	X	X		H	L	L
A3<B3	X	X	X		L	H	L
A3=B3	A2>B2	X	X		H	L	L
A3=B3	A2<B2	X	X		L	H	L
A3=B3	A2=B2	A1>B1	X		H	L	L
A3=B3	A2=B2	A1<B1	X		L	H	L
A3=B3	A2=B2	A1=B1	A0>B0		H	L	L
A3=B3	A2=B2	A1=B1	A0<B0		L	H	L
A3=B3	A2=B2	A1=B1	A0=B0		H	L	H

Truth Table for IC-4 and IC-5

TABLE 2

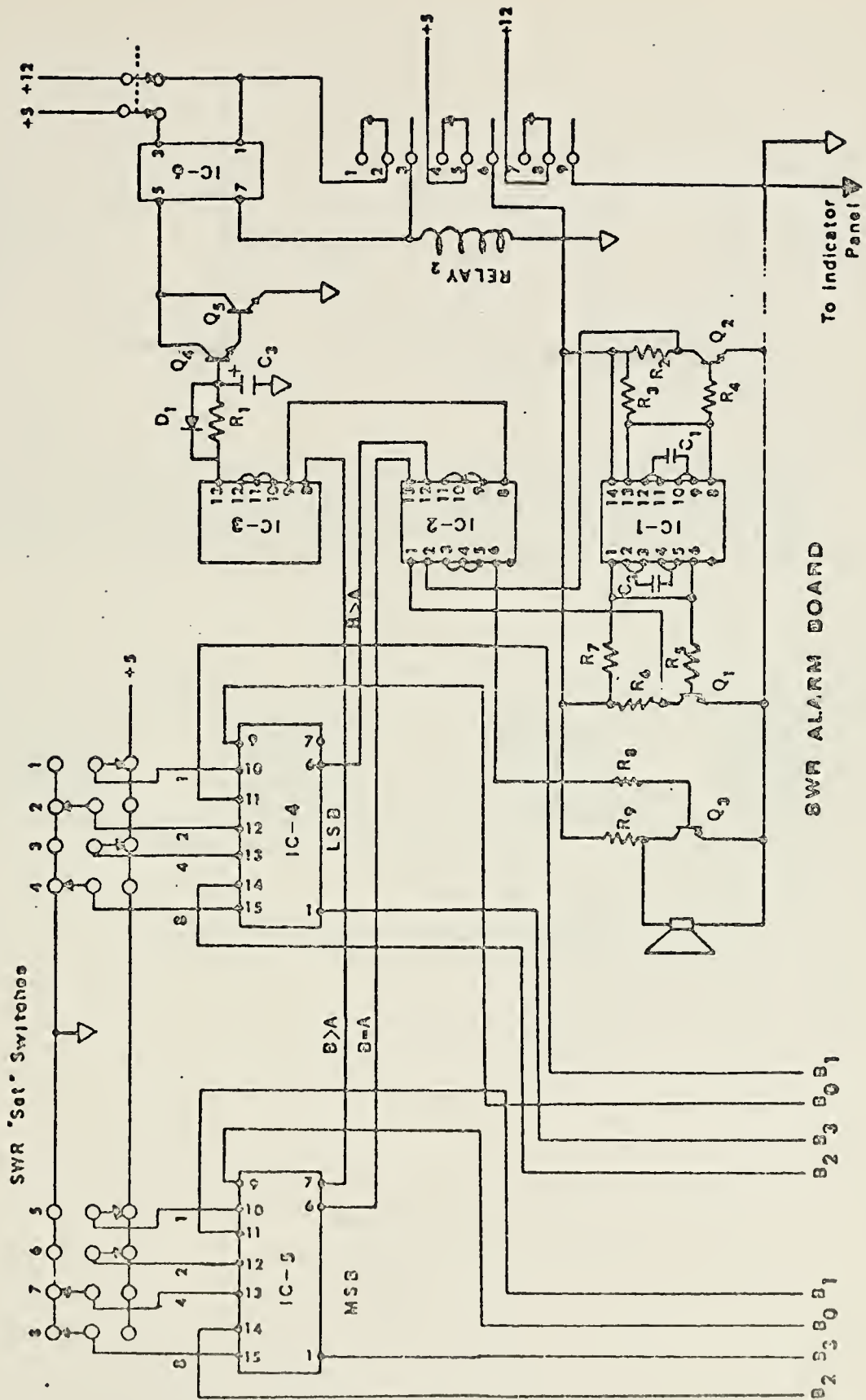
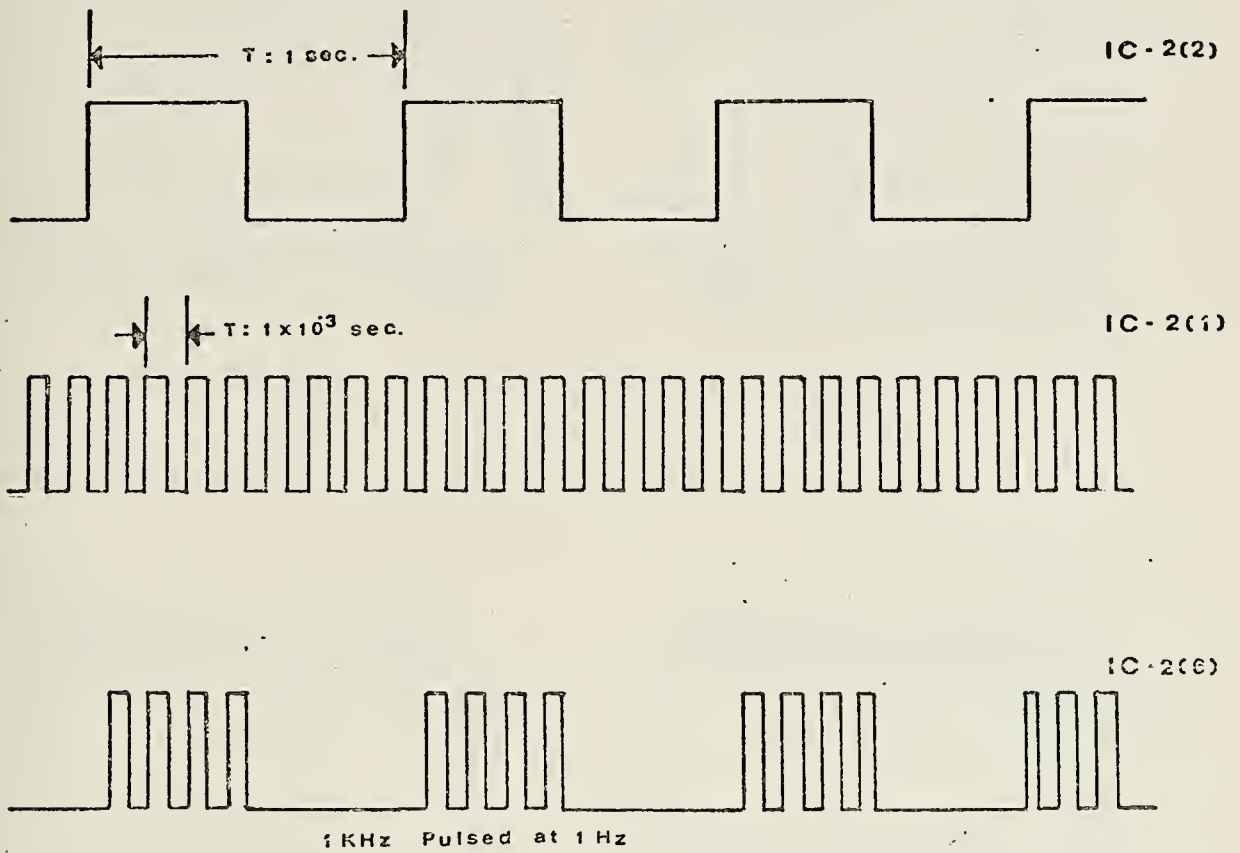
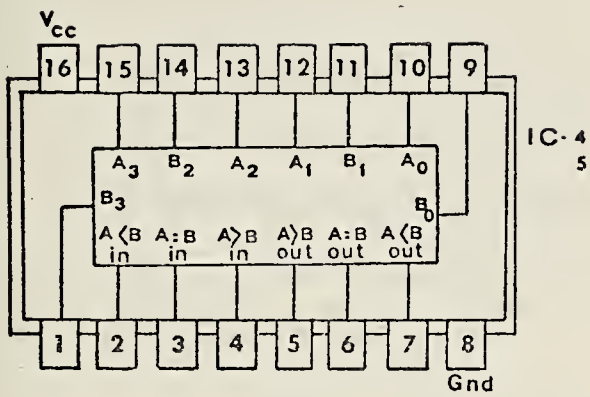


FIGURE (10)

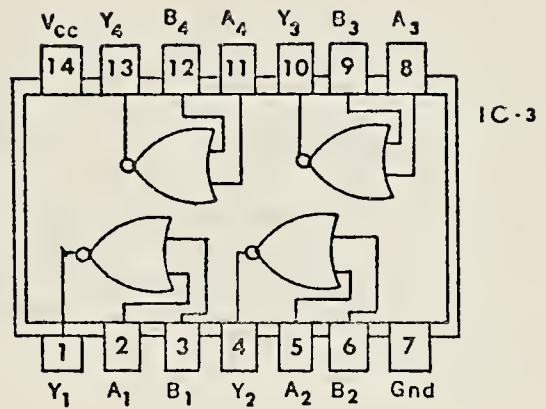


PULSE GATE RELATIONSHIPS

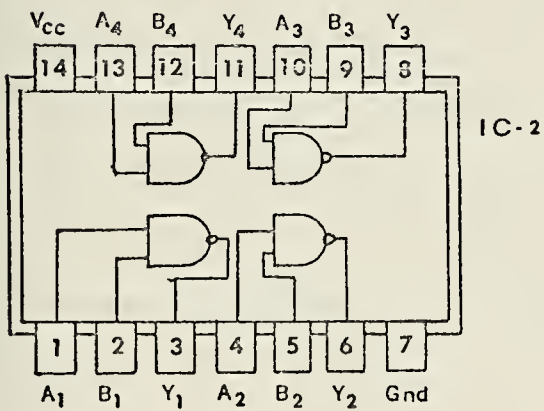
Figure (17)



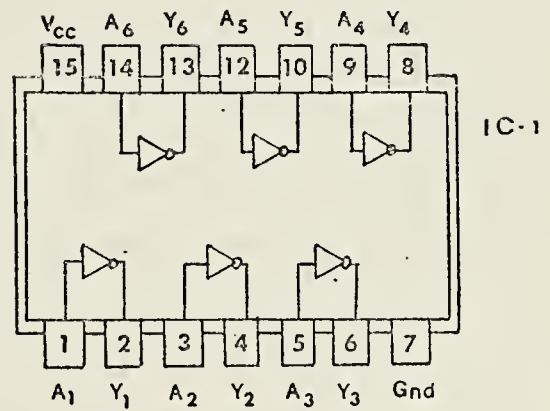
7485



7402



7400



7405

BASE CONFIGURATIONS

Figure (18)

J. ANTENNA SELECT CIRCUIT DESIGN

Figure (19) shows the schematic diagram of the antenna select circuit.

Design specifications are:

1. Capability of remotely selecting any one of N-antennas.
2. Visual indication that the N^{th} antenna has been selected.
3. HI SWR kick-down of an existing antenna and automatic connection of the affected transmitter to a dummy load.
4. HI SWR alarm light.
5. Manual reset of alarm circuits.

The antenna selector circuit was designed around an existing bank of switches and is not intended to be an optimum design. Switches $SW_{3,4,5,6}$ and 7 are mounted on a common mainframe with mechanical interlocks which prevent more than one switch to be depressed at a time.

Referring to figure (19), with switches SW_{3-7} in the "normal" position (normal is defined as no-antenna selected mode), +12 volts is passed through SW_2 to pin 2 of all antenna select switches. With all of the antenna select switches in the normal position, the +12 volts passes through each of the switches in a series mode and is connected to antenna relay "D" which energizes a multiple position antenna relay. The multiple position antenna relay connects the transmitter output to the dummy load and illuminates the DUMMY LOAD light. When any one of the antenna selector switches is depressed the series connection enabling the dummy load circuit is opened and the respective antenna relay energizes the multiple antenna switch connecting the transmitter to the desired antenna.

As long as there is no HI SWR condition, the selection of any antenna is as described above. If a HI SWR condition occurs a signal from the SWR alarm board through SW_1 energizes SW_2 . Energizing SW_2 opens the

+12 volt line supplying power to the antenna select switches and the multiposition antenna relay. When $SW_{2(a)}$ opens, $SW_{2(b)}$ closes supplying +12 volts to the "D" relay energizing the dummy load circuit and illuminating the dummy load light. Diode D_2 prevents the +12 volts from $SW_{2(b)}$ from being coupled to the antenna select switches and energizing an additional antenna relay. Once the HI SWR conditions occurs, relay R_2 , figure (16) of the SWR alarm board is locked in. This prevents the alarm indications to return to normal until the alarm circuit is manually de-energized by opening SW_1 . Provided the HI SWR alarm has cleared, opening SW_1 de-energized SW_2 , closing the "a" contacts and allowing normal operation to be resumed.

The use of the antenna select function allows a transmitter to utilize a single run of coaxial cable from the transmitter to the multiposition antenna switch, located in the vicinity of the antennas. This capability reduces the cost of installation and the problems normally associated with running a large number of cables from various antennas to a common transmitter site. The HI SWR Lock-in ensures that any alarm condition which occurs is noted by the operator. This function eliminates the possibility that an alarm occurs for a finite time then clears while the operator is engaged in other work, or out of the area. Figure (20) shows a typical installation using five antennas.

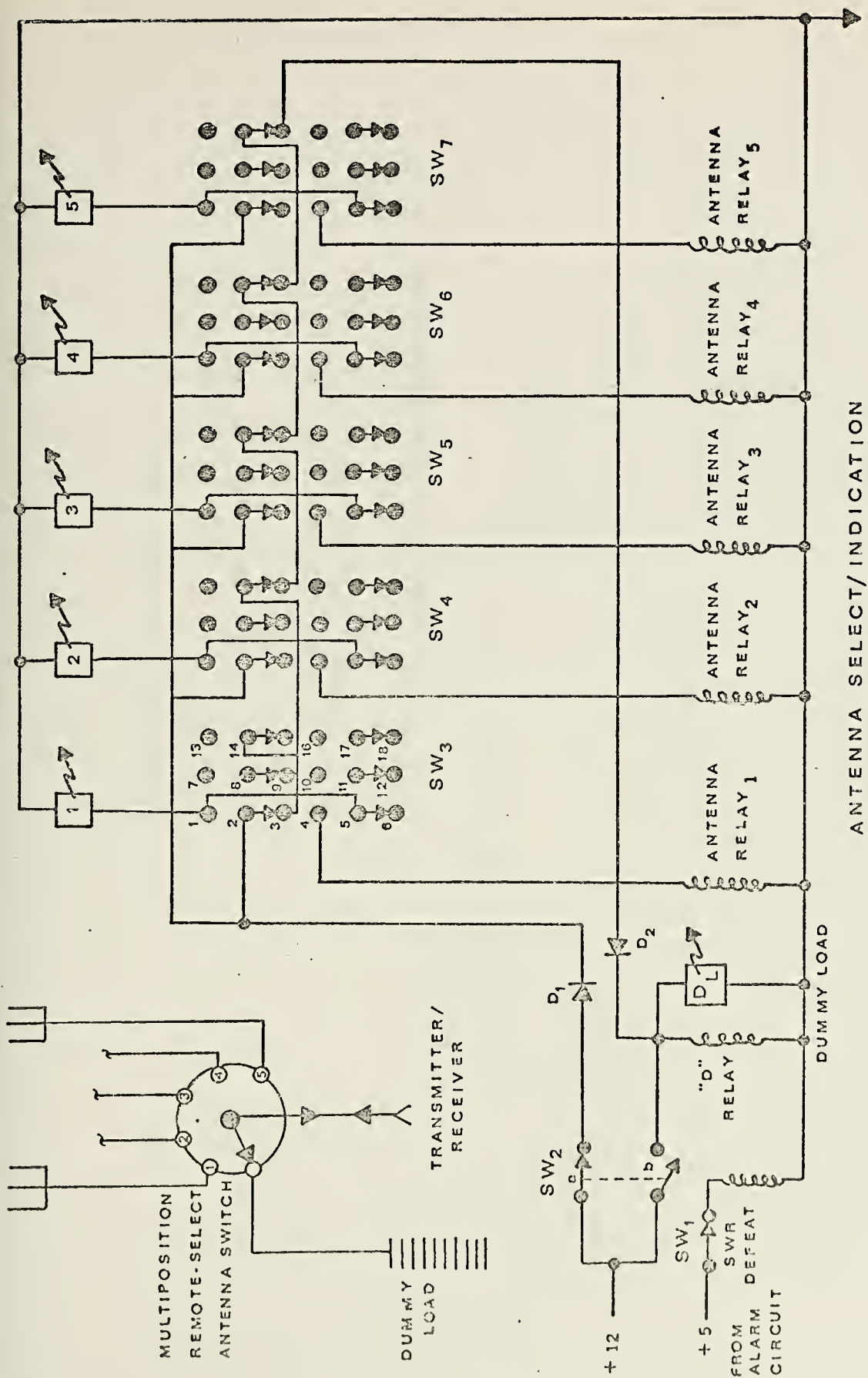


Figure (19)

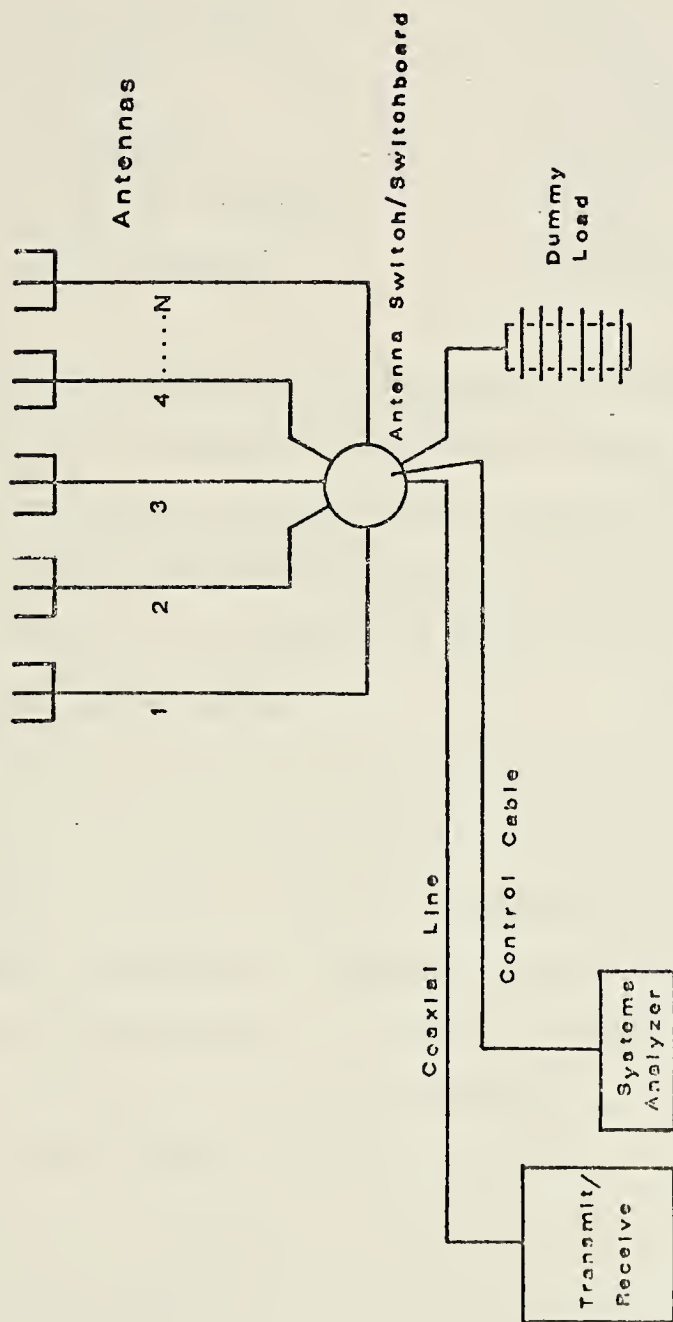


Figure (20)

K. FREQUENCY COUNTER DESIGN

The frequency counter used in the systems analyzer is an adaptation of commonly used counters. The design specifications for the counter are:

a. Frequency Range	10 Hz to 50 MHz
b. Accuracy	± 1 digit
c. Sensitivity	250 millivolts
d. Time Base Frequency	1 MHz
e. Input Impedance	Greater than 1 Megohm

Figure (21) shows a block diagram of the frequency counter. Referring to figure (21), the input circuit accepts and shapes the input signal into a square wave, and then applies the signal to the first decade counter. When this counter is turned on, the pulses from the input and shaper circuits are counted in BCD logic, with each tenth pulse passing to the next decade counter.

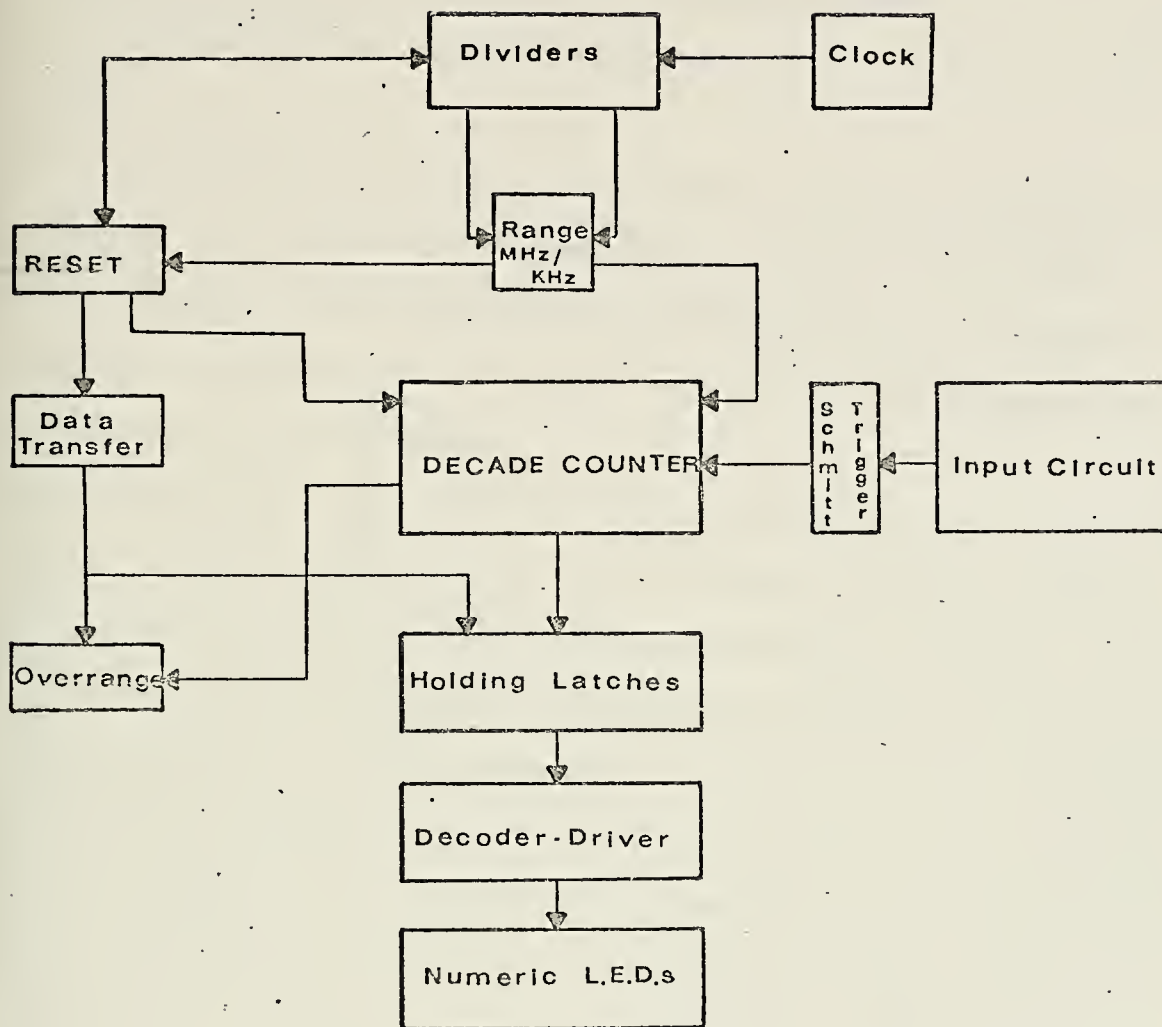
The 1 MHz clock and scaler produces a time base of 1 second or millisecond. This time base controls all of the gating circuits and determines the overall accuracy of the counter.

When a transfer pulse is applied to the holding latches, they accept the accumulated BCD count from the decade counters and hold the count at their outputs until the next transfer pulse. The outputs are connected to the decoder-drivers which translate the BCD count into a decimal number which is displayed on the numeric LEDs. Any tenth pulse from the fifth decade counter triggers the overrange detector and readout circuit to illuminate the overrange light.

For a detailed explanation of the frequency counter operation refer to Appendix I.

The frequency counter is connected to the transmission line by use of a "T" connector with a 1 picofarad capacitor. The 1 picofarad capacitor provides very light coupling to the transmission line and provides no appreciable loss.

The primary function of the frequency counter is to sample the frequency on the transmission line and display the frequency on the face panel for operator use. The frequency counter readout is additionally used in the computation of the antenna input impedance as explained in section IV (B).



FREQUENCY COUNTER BLOCK DIAGRAM

Figure (21)

L. DIGITAL CLOCK CIRCUIT

The digital clock included in the system analyzer is primarily for operator convenience. Since all logs, operating schedules, etc. are based on an acceptable time standard, it was decided to include a six digit clock.

To facilitate construction and operation accuracy, a standard clock chip was used, the MM-5314. Figure (22) shows the clock schematic. Line voltage is rectified and filtered for operating d.c. voltages. A tap on the full wave bridge provides a 60 cycle ripple voltage which is used for frequency reference.

The output of the MM-5314 is time multiplexed and fed directly to the numeric LEDs. Transistors Q_{1-7} are line drivers for the LED segments, Q_{8-13} are select drivers which determine which LED is energized. All line drivers are continuously fed data from the MM-5314, while only one select driver at a time is energized. The internal logic of the MM-5314 energizes the correct select driver allowing the data on the line drivers to be displayed. By utilizing a 1 KHz repetition rate, the digits appear to be continuously illuminated. An internal time base is available for system use by coupling out across R_{26} through C_6 . This timing base can be used to control the internal time base of the MM-5314 by the addition of transistor Q_{14} . An external time signal, such as WWV can be coupled into the MM-5314 to provide a sync with a known reference time source. This provision was not included in the construction of the digital clock.

Three momentary-make switches located on the face panel control the time setting of the clock. SW_1 advances the hours on the clock at a rate of one hour per second. SW_2 advances the minutes indication at a rate of one minute per second. SW_3 provides a holding capability. When depressed, SW_3 holds the readout of the clock constant, allowing no time

advance. This is used to hold the clock at a preset time until a time check is made. Upon releasing SW_3 the clock continues time indication from the preset time entered with SW_1 and SW_2 . The power supply for the clock is independent of the power supplied to the systems analyzer. This allows the power to the analyzer to be secured or interrupted without affecting the clock. Should the power to the clock be lost, the clock will not hold time. When power is restored, the clock will indicate a random time with part or all of the digits blanked-out. The blanking is overridden when both SW_1 and SW_2 are used to set in a new time.

By utilizing an external 60 cycle signal source, the clock can be wired such that upon loss of power only the digit illumination is lost. The clock picks up a battery supply and retains the time until the power supply is re-energized and the digits illuminated. This function is included in the second generation model.

M. POWER SUPPLY DESIGN

The current demand of this equipment is high due to the large number of elements employed. Each numeric LED draws a maximum of 140 milliamps and there are twenty numeric LEDs in the display. The nominal current per DTL/TTL chip is 10 milliamps, there are a total of 70 chips in the unit. The combination of the numeric LEDs and the chips dictate a current capability of at least 3.5 amps at 5 volts for operation. The operational amplifiers and the analog-to-digital converters operate at ± 15 volts at ± 0.8 amps. +100 volts is used for overrange indication and requires 3 milliamps for operation. The combined power requirement for the equipment is 42 watts.

In order to maintain a reasonable operating component life-time, a 5 volt, 5 amp power supply, a ± 15 volt, 1 amp power supply, and a

5 volt, .8 amp., +15 volt .8 amp supply were designed. The design of the power supplies is straight forward and requires little explanation. Figure (23) shows a block diagram of the power supplies. Figures (37) and (38) in Appendix II shows the schematic diagrams of the power supplies. Due to space limitations and heat dissipation requirements, the power supply was constructed as a separate unit and power supplied to the equipment mainframe via a power cable. The power supplies are combined on a single chassis in Appendix II. Metering of the power supply voltages is accomplished by a single meter located on the supply face panel. Figures 52 and 53 show the constructed power supplies.

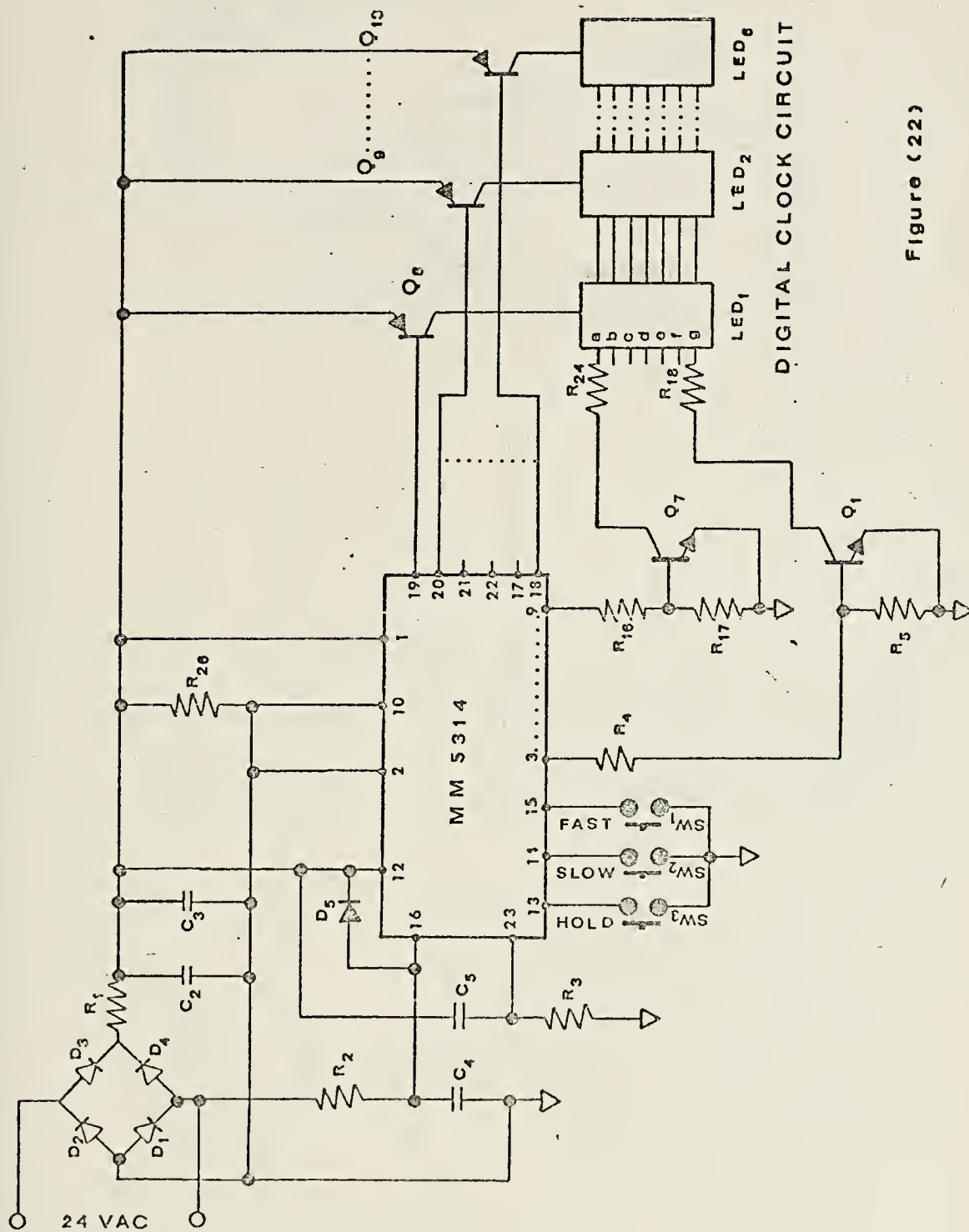


Figure (22)

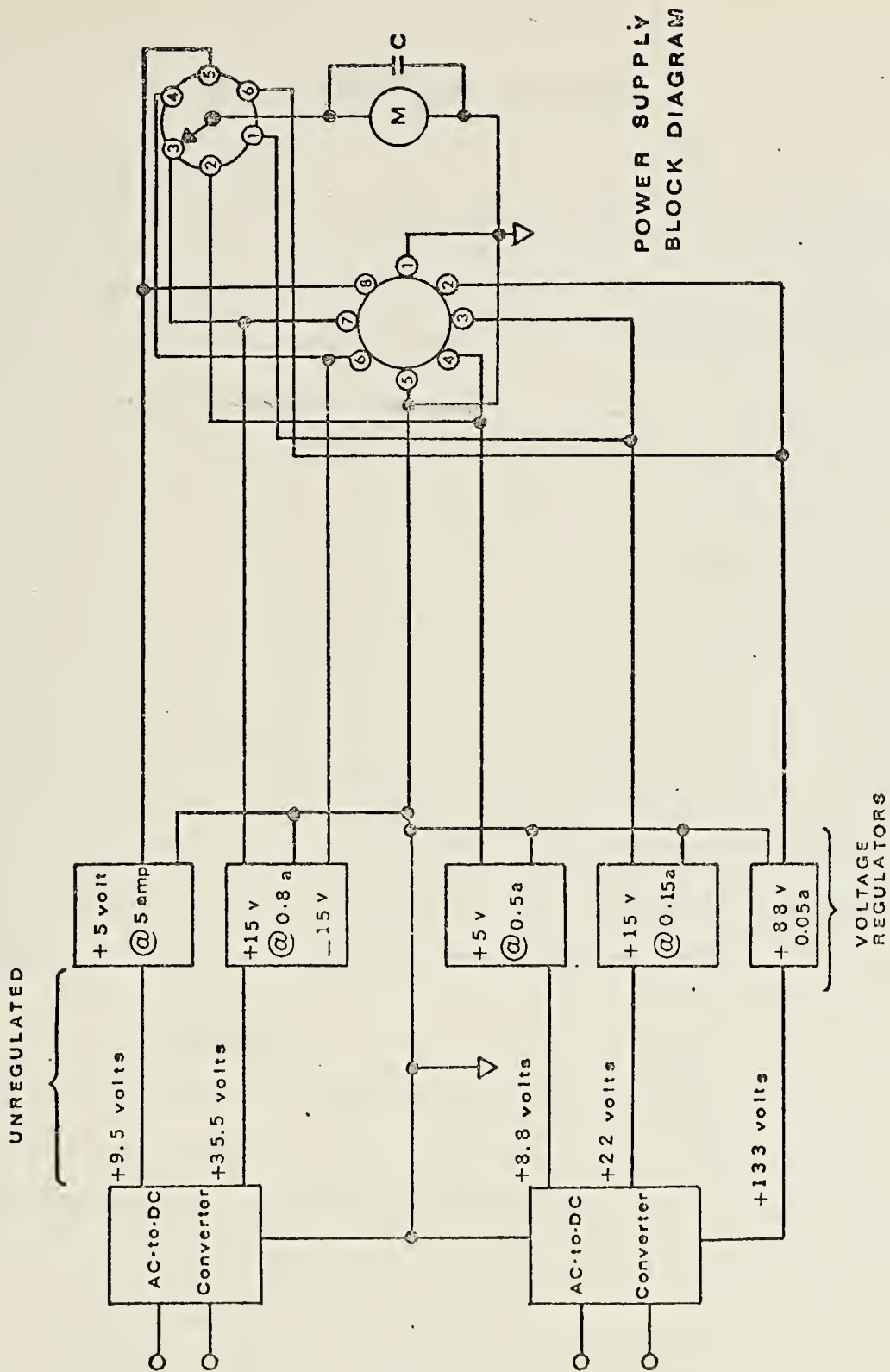


Figure (23)

III. FABRICATION AND TESTING

A. MECHANICAL FABRICATION

The major considerations involved in the physical construction of the prototype equipment were cost, ease of circuit modification without requiring wiring modifications, accessibility of circuits for testing, and availability of materials.

Several configurations were considered. A mainframe with mounted card sockets was selected as the most flexible for the system analyzer and a mainframe with hard-wired circuit boards for the power supply. Figure (46) shows the analyzer mainframe (with boards removed), figure (53) shows the power supply (with boards attached). Display cards are mounted in vector sockets located on the mainframe extension. All logic cards are mounted vertical to the mainframe behind the display cards. Sensor inputs, test signal inputs, power plugs, and antenna control plugs are located on the rear of the mainframe for easy accessibility. Figure (39) in Appendix II shows the mainframe socket interconnections.

B. LOGIC BOARD FABRICATION

Early in the project formulation, it became apparent that single sided boards were not suitable unless considerable wire runs were made for interconnections in addition to the printed wire runs. It was decided to utilize double sided boards as an obvious means to eliminate the wire runs. This resulted in additional problems. No facilities are available for plating through the board "holes" to provide continuity between upper and lower sections of the board. For connections which were clear of sockets, the holes could be designed such that a lead of a resistor,

capacitor, etc., passed through the hole. However for high density packaging, connections were required between the upper and lower portions of the circuit boards at the socket pins. After some experimentation with different types of sockets, it was discovered that by removing the lower retaining strip from the Texas-Instruments Low-Profile sockets that once the lower side solder connections were made, the socket could be lifted off the pins by gently prying them up. With the socket removed and the pins exposed, the upper side of the board could be soldered and the socket form replaced over the pins and cemented in place. While the procedure is time consuming, it proved to be the most effective means of attaching the sockets to double sided boards and without plated holes.

Soldering components to the boards was a minor problem. With high density packaging, etched lines and contact points were located close together. Direct soldering to the copper board required high soldering-iron heat (47 watts). This high heat resulted in "lifting" of the copper from the substrate. Use of a smaller iron resulted in cold solder joints. The problem was resolved by using a tin-plating solution. When the etched board is placed in the hot tin solution, tin-plate, approximately 60 microns thick, is deposited on the copper. This tinning enables good solder joints to be made with a 27 watt iron.

Figures (54) through (62) in Appendix IV show the upper and lower card sections with pin identification for the boards used in the systems analyzer.

C. SUB-SYSTEM TESTING

Each board was tested on the Digital-Test Set under static conditions prior to insertion on the equipment mainframe. All final calibration and testing was done on the equipment mainframe. The system analyzer can be

broken into five basic sub-assemblies:

1. Frequency Counter
2. Forward/Reflected Power Indication
3. SWR Indication
4. SWR Alarm Circuits
5. Digital Clock

Each sub-system was wired into the mainframe, tested, calibrated, and retested under simulated input conditions. Upon completion of the mainframe, all sub-assemblies were tested under controlled conditions utilizing low power r.f. signals. Final testing consisted of low and medium r.f. power, on-the-air tests using multiple antennas and mismatched terminations.

D. FREQUENCY COUNTER TESTING

Figure (24) shows the test set-up required to test and calibrate the frequency counter. The reference frequency counter and signal generator were energized 24 hours prior to testing/calibration. The test frequency was energized for one hour prior to testing and calibration.

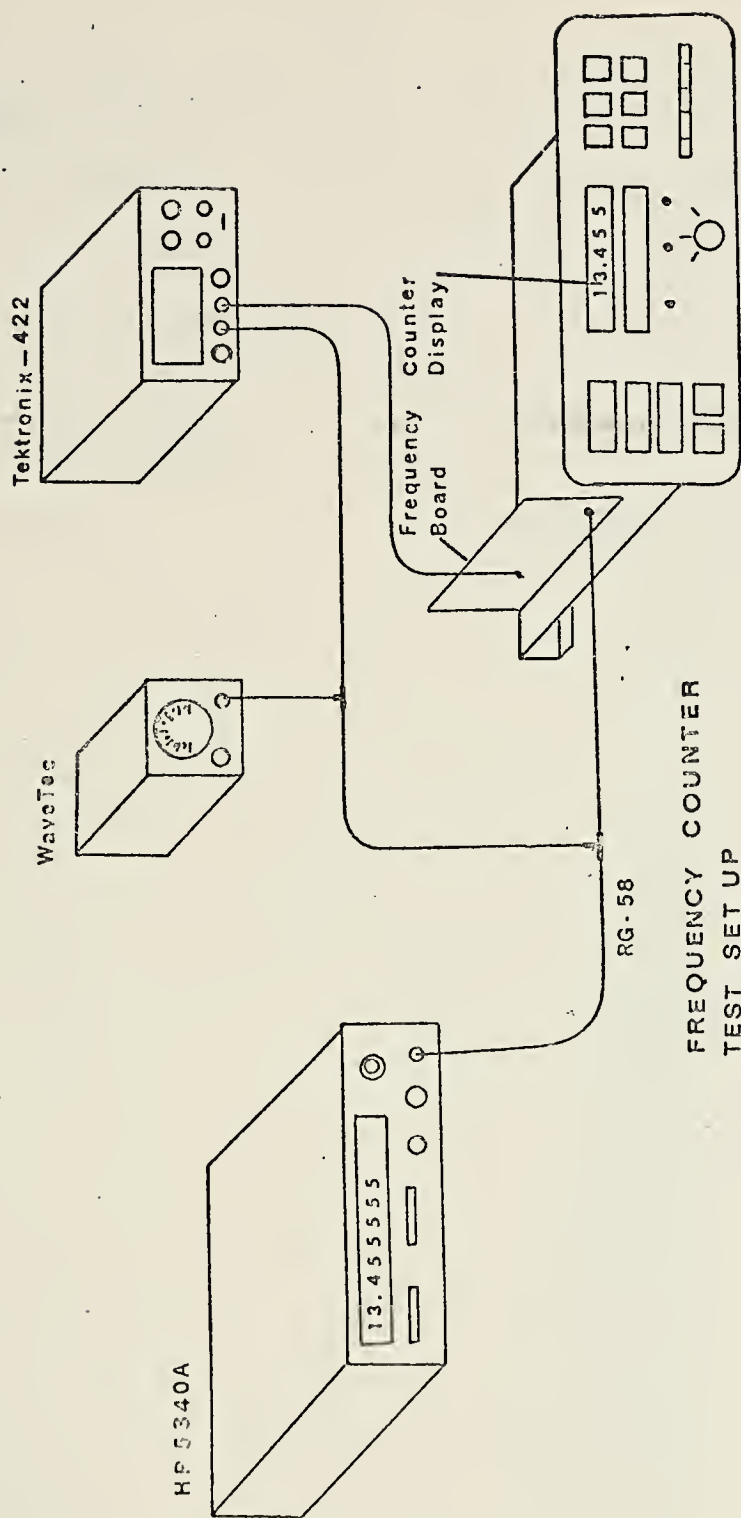


Figure (24)

Measured Data:

1. Dip voltage 5.07 volts
2. Shaping circuit voltage 15.53 volts
3. Internal Clock/Oscillator 1,000,000 Hz
- Drift rate per 24 hours 1 Hz
- Drift rate for first 30 min. after
initial power-on 180 Hz

4. Input Voltage vs. Frequency

Voltage _{p-p}	Frequency (Hz)
0.8	5
0.5	10
0.4	20
0.35	50
0.35	100
0.3	1,000
0.28	5,000
0.28	10,000
0.26	50,000
0.27	100,000
0.25	250,000
0.27	500,000
0.3	1,000,000
0.33	5,000,000
0.38	10,000,000
0.37	20,000,000
0.4	30,000,000
0.4	35,000,000
0.48	40,000,000
0.88	44,000,000
erratic operation above 44 MHz.	

5. Frequency Accuracy

<u>Reference Counter (Hz)</u>	<u>Test Counter (Hz)</u>
1	no count
5	6
10	10
20	21
40	40
80	81
100	101
500	500
1,000	1,000
5,000	5,000
10,000	10,000
50,000	50,000
99,999	100,000
500,000	500,000
1,000,000	1,000,000
2,755,999	2,756,008
5,555,555	5,555,562
10,000,000	10,000,003
20,500,500	20,500,525
30,000,000	29,998,999

E. FORWARD/REFLECTED POWER BOARD TESTING

Figure (25) shows the test set-up for mainframe static testing of the forward/reflected power board.

Test Data:

Reference Voltages (volts)			Visual Power Indication	
	Forward	Reflected	Forward	Reflected
1.	0.000	0.000	000	00.0
2.	.005	.002	005	03.0
3.	.010	.005	010	05.0
4.	.020	.007	020	07.0/07.2*
5.	.050	.010	050	10.0
6.	.100	.015	101	14.4
7.	.150	.020	151	19.6
8.	.200	.025	199	25.1
9.	.250	.027	249	27.2
10.	.300	.030	300	30.0/29.9*
11.	.350	.035	352	35.0
12.	.400	.040	399	40.1
13.	.450	.045	450	45.5/45.2*
14.	.475	.050	474	50.0/49.9*
15.	.555	.055	555	55.0/54.8*
16.	.700	.075	698	76.0
17.	.757	.077	758	76.8/77.0*
18.	.835	.080	835	80.2/79.9*

* Indicates display changing state during read-time.

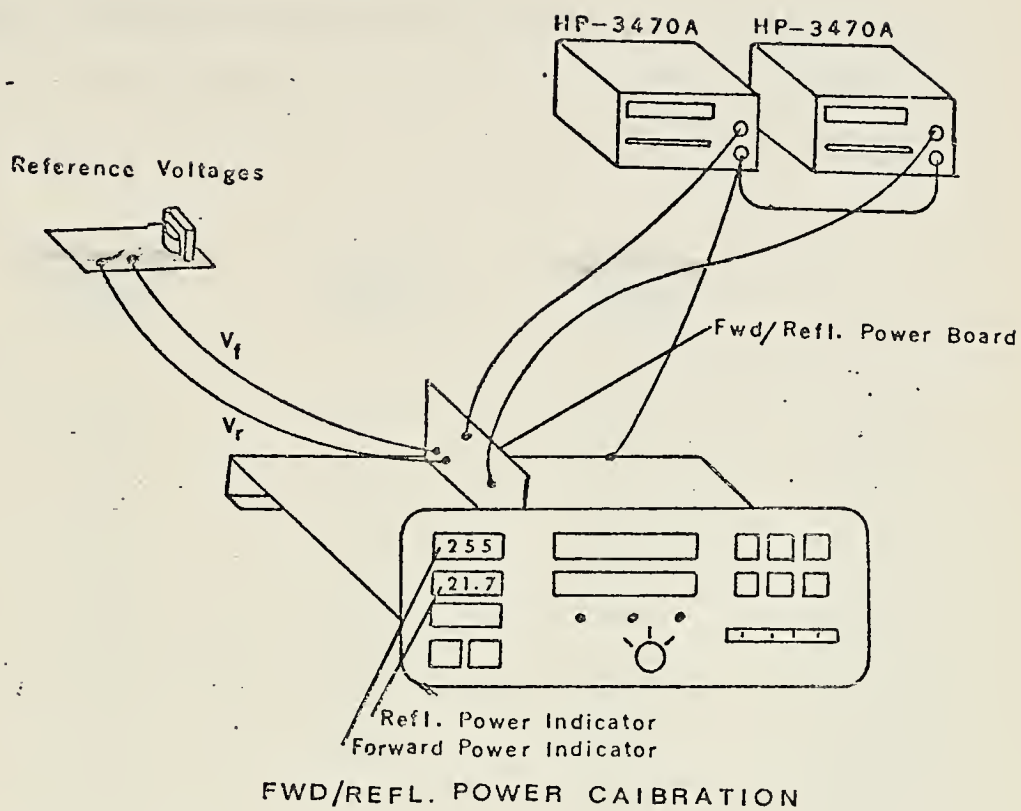


Figure (25)

F. SWR INDICATION BOARD TESTING

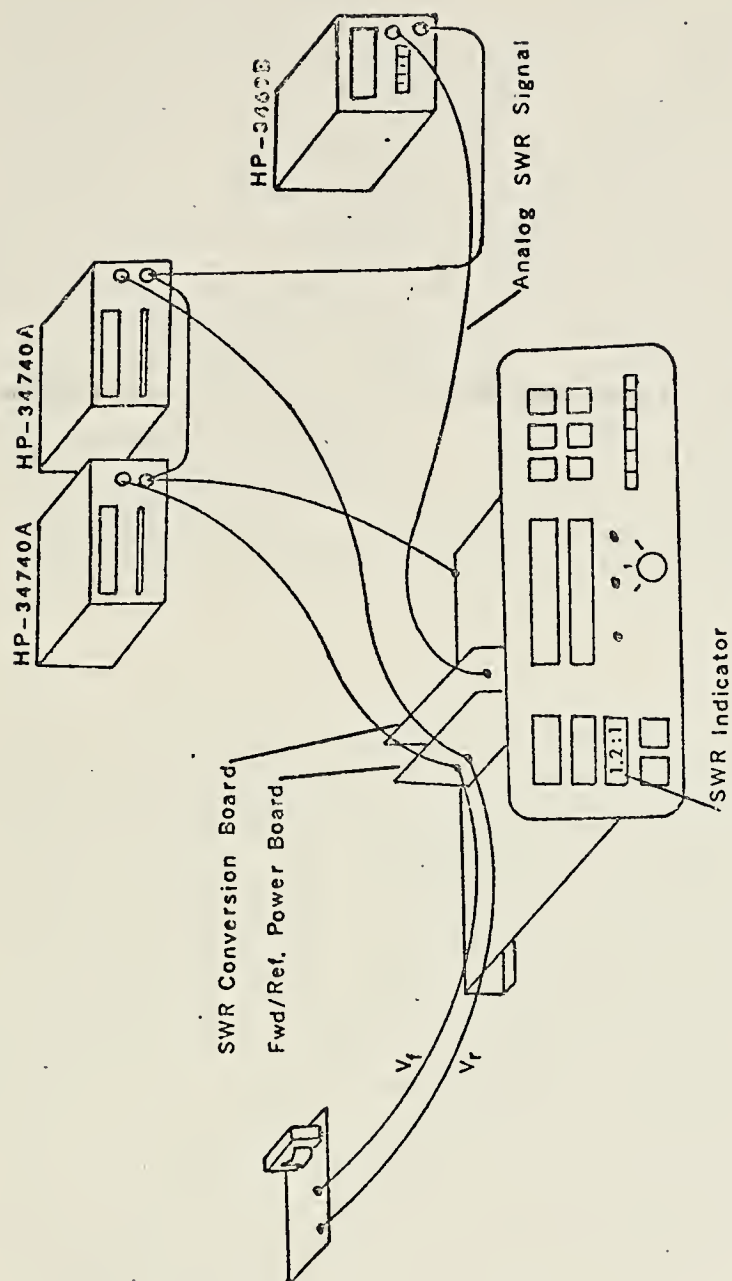
Figure (26) shows the test set-up for testing the SWR board. For testing of the SWR board, the forward/reflected board was left on the mainframe. Input voltages are selected off the sensor curve, figure (4). Power indications should compare with the linearized curve, figure (4), curve "B"

SWR Board Data:

	Forward Voltage Input	Reflected Voltage Input	Forward Power Indicated	Reflected Power Indicated	SWR
1.	.140	0.00	101	00.0	1.0:1
2.	.140	0.02	101	11.0	2.0:1
3.	.140	0.05	100	25.2	3.2:1
4.	.140	0.08	101	38.4	4.3:1
5.	.140	0.10	100	57.5	7.4:1
6.	.140	0.12	101	78.0	6.2:1*
7.	.000	0.03	0	10.2	0.0:1
8.	.030	0.03	011	10.0	9.1:1
9.	.050	0.03	025	10.3	4.6:1
10.	.075	0.03	035	11.1	3.4:1
11.	.100	0.030	059	10.8	2.4:1
12.	.125	0.030	085	10.9	2.1:1
13.	.140	0.030	100	11.0	2.0:1
14.	.160	0.030	114	10.7	1.8:1
15.	.140	0.010	102	04.2	1.5:1

* Overrange indicator lamp lighted.

Figure (27) is a graph of the output of the forward power linearizing circuit and the reverse power linearizing circuit versus sensor voltage output.



SWR BOARD CALIBRATION.

Figure (26)

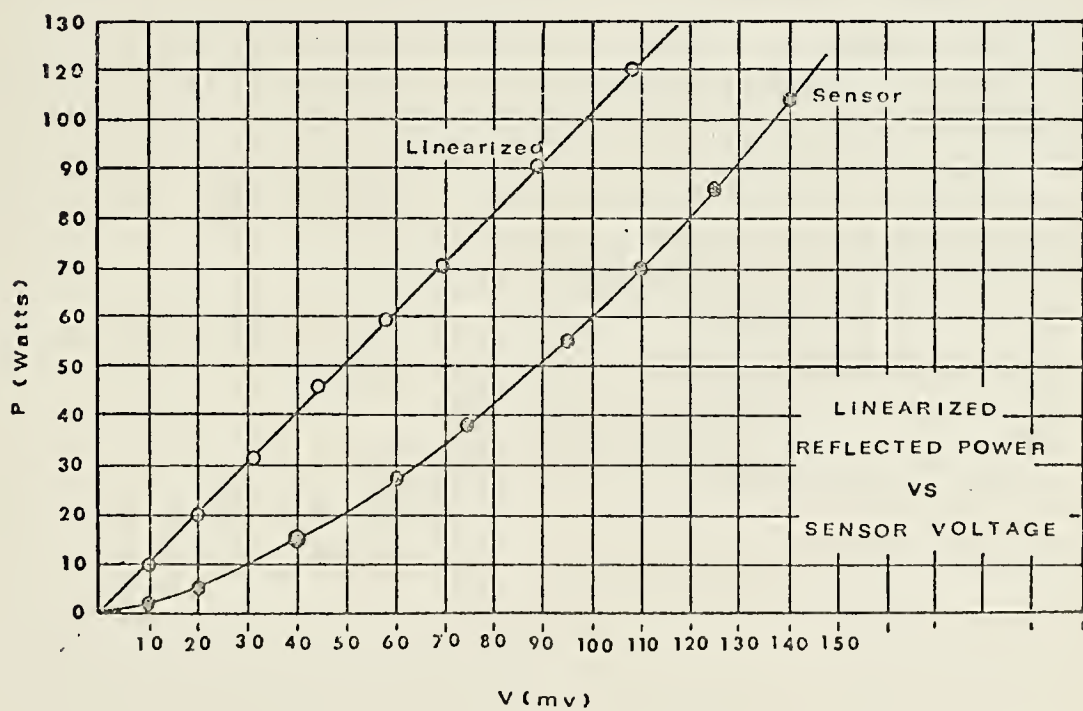
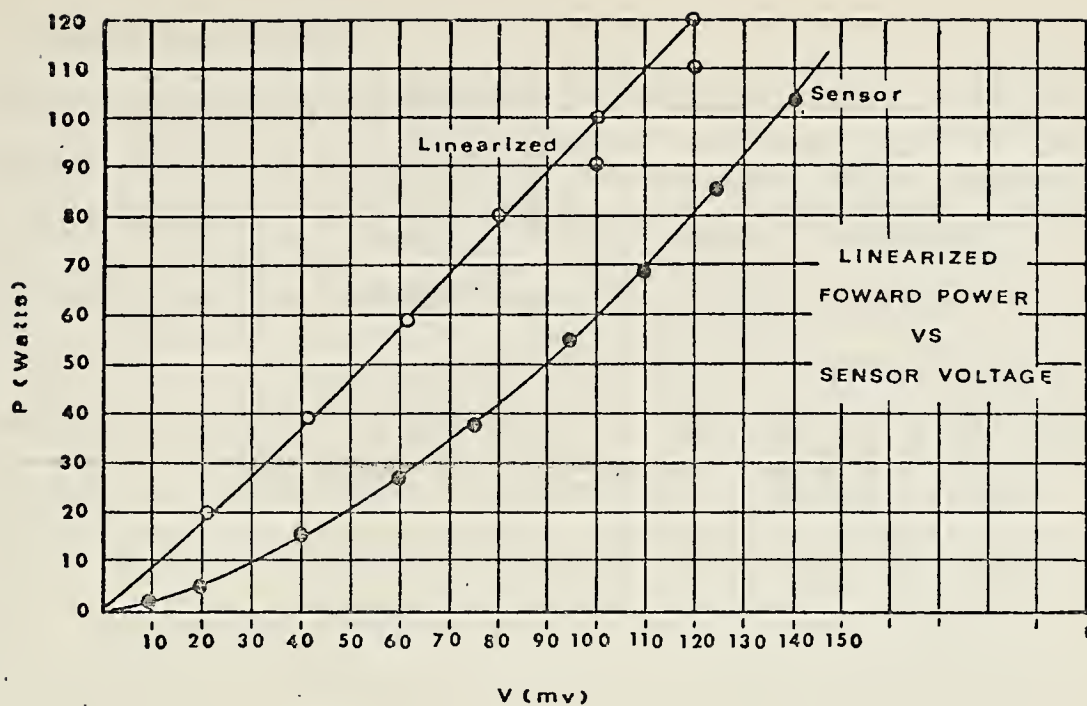


Figure (27)

G. SWR ALARM CIRCUIT TESTING

Testing of the SWR alarm board utilized the same test set-up as the SWR indicating board tests. The forward/reflected power indicating board and the SWR conversion board were left on the mainframe. The reverse power signal input was set at 30 millivolts for all tests, and the forward power signal voltage was varied. The SWR limit switches on the SWR alarm board were set to 2.0 (0010-000), 2.5 (0010-0101), 3.6 (0011-0110), 4.2 (0100-0010), 5.5 (0101-0101), 7.0 (0111-000), 8.3 (1000-0011), and 9.9 (1001-1001), and the forward signal voltage varied until the alarm triggered. The indicated SWR was recorded at the trip point. Observations were made after each trip point had been reached as whether or not the visual alarm, audible alarm, and antenna kick-down occurred.

S.W.R. TRIP POINT TEST DATA

DECIMAL S.W.R.	BINARY SWITCHES S_{1-8}		OBSERVED TRIP POINT
2.0	0010	0000	2.1 : 1
2.5	0010	0101	2.6 : 1
3.6	0011	0110	3.6 : 1
4.2	0100	0010	4.2 : 1
5.5	0101	0101	5.4 : 1
7.0	0111	0000	7.2 : 1
8.3	1000	0011	8.4 : 1
9.9	1001	1001	9.7 : 1

H. DIGITAL CLOCK TESTING

Testing of the digital clock consisted of monitoring the time indicated on the clock and comparing the time with the numeric readout of WWV as copied by the NPG time standard. Over a 48 hour period the digital clock indicated a one-second difference. Based on a 48 hour test, the daily error is 0.5 seconds per 24 hour period. This error correlates the 3 minutes and 2.4 seconds per year.

I. SYSTEM TESTS AND RESULTS

Final testing of the systems analyzer utilized active sources, random lengths of terminated transmission line, and three radiating structures. Figure (28) shows the test set-up and equipment identification. Due to limitations of the transmitter used in the testing, a continuous check (systematic frequency/power selection), was not possible. Four frequencies were checked at three different power levels each. Each test was conducted with six different terminations.

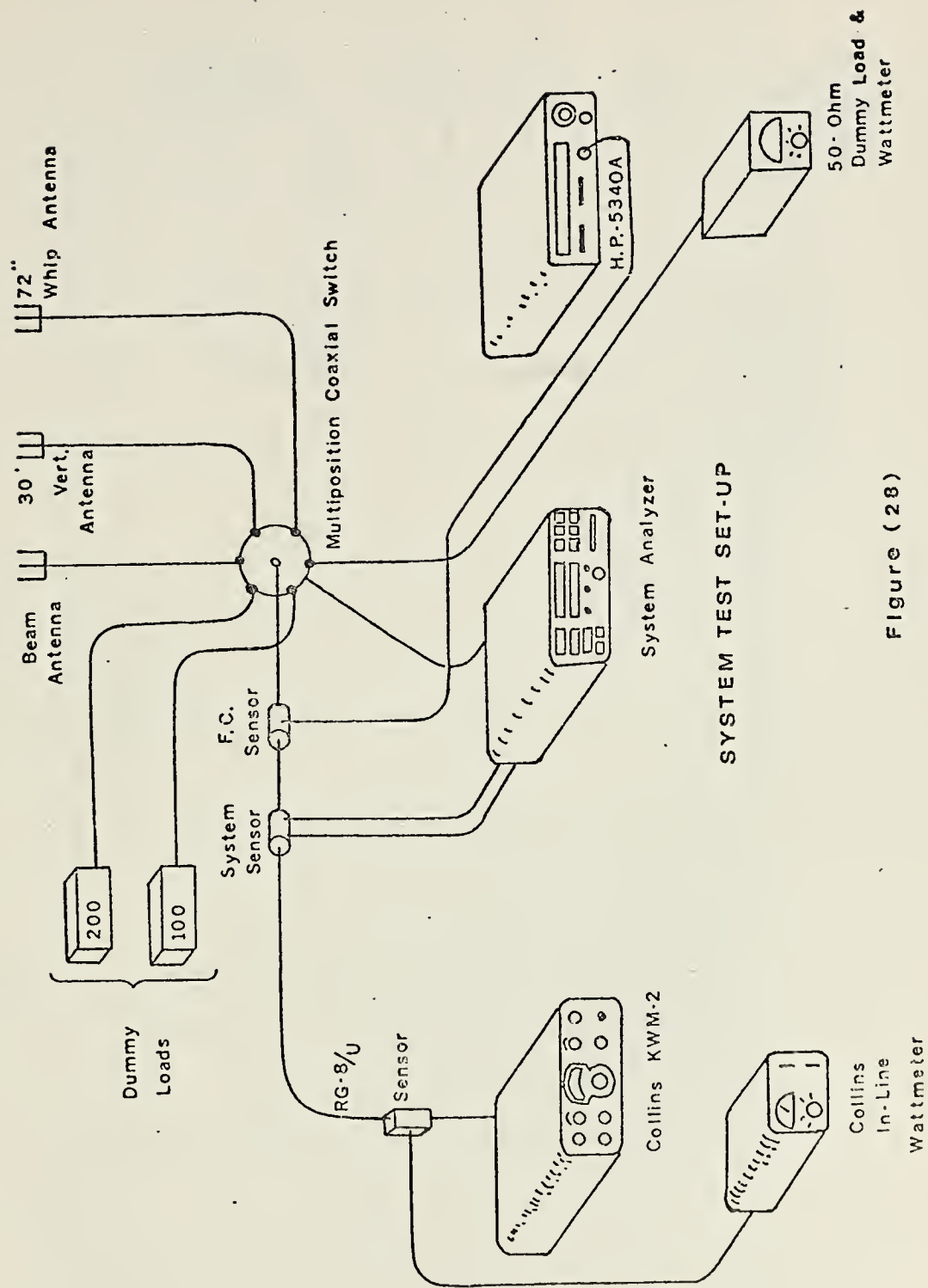


Figure (28)

ANTENNAS: 1) SWAN 30 Ft. Trapped Vertical, Pre-Tuned For Min. Reflected Power At Test Freqs.
 2) SWAN Center Loaded Mobile Whip Over a 121 sq.ft. Ground Plane
 3) HYBRID "QUAD" BEAM

TEST DATA																		
FREQ. (MHz)	POWER (WATTS)	Collins Wattmeter		Recorded Power			CALCULATED SWR	OBSERVED SWR	FREQUENCY (MHz)		50 OHM LOAD	100 OHM LOAD	200 OHM LOAD	BEAM ANTENNA	30 FOOT VERTICAL	72 INCH TUNED WHIP	COMMENTS	
		P ₁	P ₂	P ₁	P ₂	P ₃			HP-5340A	TEST SET								
3975	20	21	2	21	0	21	0	1.9	1.0	397500	3.975	X					SWR=1.0	
"	"	19	4	20	2.5	2.5	2.7	2.1	2.1			X					SWR=2.0	
"	"	19	8	20	6.1	6.1	4.7	3.7	3.7			X					SWR=4.0	
																	NOT USED AT THIS FREQUENCY	
50	50	55	5	52	1.0	1.0	1.9	1.2	1.2			X					SWR=1.0	
"	"	53	0	51	4.1	4.1	2.3	1.8	1.8			X					SWR=2.0	
"	"	53	15	51	19.8	19.8	3.3	3.8	3.8			X					SWR=4.0	
100	100	98	5	101	2.0	2.0	1.6	1.2	1.2			X					SWR=1.0	
"	"	95	15	100	15.1	15.1	2.3	2.2	2.2			X					SWR=2.0	
"	"	95	35	100	38.3	38.3	4.1	4.2	4.2			X					SWR=4.0	
7255	20	20	2.1	22	1.1	1.1	1.9	1.3	1.3	725501	7.255	X					SWR=1.0	
"	"	20	3	21	2.3	2.3	2.2	1.9	1.9			X					SWR=2.0	
"	"	20	10	21	5.6	5.6	5.8	3.3	3.3			X					SWR=4.0	
"	"	19	0	19	2.3	2.3	1.0	1.5	1.5					X				
"	"	20	2	19	2.1	2.1	1.9	2.2	2.2							X		
50	50	43	3	50	1.1	1.1	1.6	1.2	1.2			X					SWR=1.0	
"	"	48	7	49	6.8	6.8	2.2	2.0	2.0			X					SWR=2.0	
"	"	49	20	51	19.5	19.5	4.5	4.3	4.3									

SWR Computed From
 Impedance Equation: $SWR = \frac{1 + \left| \frac{Z_L - Z_0}{Z_L + Z_0} \right|}{1 - \left| \frac{Z_L - Z_0}{Z_L + Z_0} \right|}$

TEST DATA													
FREQ. (MHZ)	POWER (WATTS)	Collins Wattmeter			Recorded Power			CALCULATED SWR	OBSERVED SWR	FREQUENCY		50-OHM LOAD	100-OHM LOAD
		P _i	P _r	P _t	P _i	P _r	P _t			HP-5340A	TEST SET		
7.255	95	95 #	1	97	0			1.22	1.0	7.25499	7.255	x	
	"	95 #	8	94	7.6			1.81	1.8			x	
	"	95 #	36	95	35.3			4.2	4.3				
	"	95 #	10	94	11.6			1.96	2.1				
	"	95 #	8	94	9.0			1.81	2.0				
14.255	20	20	2	18	0			1.92	1.0	14.2550	14.255	x	
	"	20 +	2	18	2			1.92	2.1			x	
	"	20 +	6	19	5.7			3.42	3.5				x
	"	20 -	2	18	1.2			1.92	1.7				
	"	20	6	18	5.5			3.42	3.5				
	"	20 +	5	18	5.6			3.2	3.5				
80	80	80	2	79	1			1.37	1.4			x	
	"	80	10	78	8.7			2.09	2.1				
	"	80	28	81	27.3			3.89	2.8			x	
	"	80 -	6	80	4.5			1.75	1.6				
	"	80 -	20 +	79	18			3.65	2.9				
	"	80 -	22	79	22			3.2	3.3				
28.614	20	20	0	21	1			1.0	1.0	28.6143	28.614	x	
	"	20	2	21	2.2			1.92	1.9			x	

Approximate Value

+ Meter Slightly Above or Below mark

TEST DATA													
FREQ (MHZ)	POWER (WATTS)	Collins Wattmeter			Recorded Power			OBSERVED SWR	FREQUENCY (MHZ)		50-OHM LOAD	100-OHM LOAD	200-OHM LOAD
		P _t	P _r	P _e	P _t	P _r	P _e						
28.614	20	18	6	19	6.2	3.7	3.9		28.6148	28.614	X		X
	20	18	2	19	2.0	2.0	1.8						X
	20	18	2	18	2.1	2.0	2.0						
	20	18	4	18	4.3	2.8	2.9						
	80	82	2	84	0.5	1.3	1.0				X		
	80	82	8	84	8.7	1.9	2.1					X	
	20	82	26	83	22.6	3.6	3.4						
	80	82	6	84	6.5	1.7	1.6					X	
	80	82	12	85	11.4	2.2	2.2						X
	80	80 ⁺	15	83	14	2.5	2.6						X
	250 *	250 ⁺	20	255	20.7	1.8	2.0					X	
	250 *	240 ⁺	34	255	33.6	2.2	2.1						X
	250 *	250 ⁺	44	250	47.3	2.4	2.6						X
3825	50	48	20			4.4	4.5		382500	3825			X
	50	48	26			6.2	6.5						
7050	50	50	18	51	20	4.0	4.1		70505	7050			X
	50	50	25	51	27	5.8	5.9						
													X

* LINEAR USED

** TESTED OUTSIDE ANTENNA OPERATING BAND

J. COMMENTS ON TEST DATA RESULTS

The 100 ohm and 200 ohm dummy loads constructed were considered to be true values of 100 and 200 ohms at all frequencies tested. Actually there were inductive and capacitive reactances present which modified the actual value of the dummy loads as a function of frequency. The recorded values of SWR and the calculated values of SWR agree closely enough with the SWR computed using the impedance values of 100 and 200 ohms, to indicate the value of stray inductance and capacitance is small in the frequency range tested. The 50 ohm load is a commercially manufactured unit and has a resistive value of 50 ohms within the frequency bands tested.

From the results of the test data, it appears that the System Analyzer yields good results at low power levels, as well as at higher power levels. The original intent was to utilize the Collins Wattmeter as a reference source against which the System Analyzer could be measured. From the values of forward and reflected power, as read off the meter, it is apparent that there is either an inherent inaccuracy at low power levels, or the diodes used in the Collins Wattmeter have changed operating characteristics. At low power levels at low frequencies, the calculated SWR appears to be in error. Table VI lists the calculated SWR error and the recorded SWR error based on non-reactive dummy load SWR.

There were no test facilities available to determine whether the values of SWR as recorded from the three antennas used were correct. Assuming an inaccuracy at low power levels in the readings of the Collins Wattmeter, the recorded values of SWR are close to the calculated values. Table VII shows the values of SWR calculated and recorded and the percentage difference.

The testing done, and the explanations presented, have assumed a transmitting situation. It should be pointed out that the System Analyzer

can be used with receive antennas as well. From the data taken, it appears that the System Analyzer operates well at low power levels. This fact should allow it use with receive antenna arrays, etc. The total per-channel up date time on the unit constructed is 1-sec, and 1-milli-second on the recommended improved unit. By utilizing a scanning switch and a digital printer, the Systems Analyzer, conceivably, could be used to check a large number of antennas, both transmitt and receive, and automatically print out the desired data.

Persons desiring component values for the constructed circuits may obtain them by contacting LT. Patrick at SUPSHIPS, Mare Island Naval Shipyard, Vallejo, California.

Freq.	Dummy Load-SWR	Calculated SWR	Observed SWR	% Calc. Error	% Obs. Error
3.975	1.0	1.9	1.0	90	0
	2.0	2.7	2.1	35	5
	4.0	4.7	3.7	17.5	7.5
	1.0	1.9	1.2	90	20
	2.0	2.3	1.8	15	15
	4.0	3.3	3.8	17.5	5
	1.0	1.6	1.2	60	20
	2.0	2.3	2.2	15	10
	4.0	4.1	4.2	2.5	5
7.255	1.0	1.9	1.3	90	30
	2.0	2.2	1.9	10	5
	4.0	5.8	3.3	45	17.5
	1.0	1.6	1.2	60	20
	2.0	2.2	2.0	10	0
	4.0	4.5	4.3	12.5	7.5
	1.0	1.22	1.0	22	0
	2.0	1.81	1.8	10	10
14.255	1.0	1.92	1.0	92	0
	2.0	1.92	2.1	5	5
	4.0	3.42	3.5	14.5	12.5
	1.0	1.37	1.4	37	40
	2.0	2.09	2.1	4.5	5
	4.0	3.89	3.8	2.8	5
28.614	1.0	1.0	1.1	0	10
	2.0	1.92	1.9	4	5
	4.0	3.7	3.9	7.5	2.5
	1.0	1.3	1.0	30	0
	2.0	1.9	2.1	5	5
	4.0	3.6	3.4	10	15

Mean Error of Calculated SWR 27.9%

Mean Error of Observed SWR 9.7%

Table VI

Freq.	Calculated SWR	Observed SWR	% Difference	
3.975	1.9	1.0	90	
	2.7	2.1	28	
	4.7	3.7	27	
	1.9	1.2	58	
	2.3	1.8	28	
	3.3	3.8	13	
	1.6	1.2	33	
	2.3	2.2	5	
	4.1	4.2	2	
7.255	1.9	1.3	46	
	2.2	1.9	14	
	5.8	3.3	78	
	1.0	1.5	33	
	1.9	2.2	14	
	1.6	1.2	33	
	2.2	2.0	10	
	4.5	4.3	5	
	1.22	1.0	22	
	1.81	1.8	0	
	4.2	4.3	2	
	1.96	2.1	7	
	1.81	2.0	10	
14.255	1.92	1.0	92	Average % Difference 16.4
	1.92	2.1	9	
	3.42	3.5	2	
	1.92	1.7	13	
	3.42	3.5	2	
	3.2	3.5	9	
	1.37	1.4	2	
	2.09	2.1	0	
	3.89	3.8	2	
	1.75	1.6	9	
	3.65	3.5	4	
	3.2	3.3	3	
28.614	1.0	1.0	0	
	1.92	1.9	0	
	3.7	3.9	5	
	2.0	1.8	11	
	2.0	2.0	0	
	2.8	2.9	3	
	1.3	1.0	30	
	1.9	2.1	10	
	3.6	3.4	6	
	1.7	1.6	6	
	2.2	2.2	0	
	2.5	2.6	4	
	1.8	2.0	10	
	2.2	2.1	5	
	2.4	2.6	8	

Table VII

IV. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The preliminary performance test results indicate that the design criteria as specified are met by the prototype equipment. More work is required to eliminate the readout "numeric-jitter" present in the forward and reverse power indications. The jitter does not degrade the performance, but does detract from the system's visual aspect.

The tests conducted with the KWM-2 transceiver, associated dummy-loads, and antennas, indicate that the basic concept of sensing radio-frequency signals on a transmission line, digitizing the signals and displaying the numeric value accurately is feasible. The SWR circuits constructed, once properly calibrated, yielded values of SWR which had less than the expected error. It is extremely convenient to be able to see the forward power, reflected power, SWR and operating frequency visually displayed during tune-up of a transmitter, and during operation. Once operator confidence in the performance of the Systems Analyzer was established, additional checks of antennas under operating conditions indicated generally higher operating SWR levels than anticipated. Once detected, the SWR was reduced by proper adjustment of the antennas and the transmission-lines.

The author strongly feels that the development of a similar unit, suitable for shipboard installation would result in better performance of installed transmitters and antenna systems. Better performance of shipboard equipment by detecting and correcting or controlling r.f. losses which result in a higher SWR, should additionally increase the point-to-point communications of the ship, an end to which all dedicated Naval Officers are committed.

B. RECOMMENDATIONS

The circuits presented in the text of this paper were, as is any construction project, a compromise between what is desired and what is obtainable. In this case the obtainable parts were further limited to those which could be ordered through the Navy Supply System, and the delays associated with the ordering of the parts. The recommendations presented herein are those which, if parts were available, would result in an appreciable increase in circuit and/or display efficiency and accuracy.

The operation of the digital clock, SWR alarm board, and the display boards are satisfactory, and cost effective. The major area of concern is with the Forward/Reflected power circuits and the SWR detection and conversion circuits. The use of relays on the Forward/Reflected Power board to transfer the input sensor voltage to the A/D converter, associated latches and control circuitry is slow and inefficient. In theory the use of an analog calculator to compute the SWR is sufficient to do the job. In practice the error associated with the analog calculator is function of the quality of parts, tolerance, and the voltage used. Any variations, or fluctuations in component values and/or voltage can increase the errors beyond an acceptable level. Frequent calibration checks are required to ensure accurate operation. An improved multiplexer and conversion scheme is shown in figure (29). Greater input flexibility is achieved by the use of a Datel MM8 Analog Multiplexer, a total of eight inputs can be sequentially entered and converted. The MM8 eliminates the need for the second A/D converter as used in the constructed circuits. The MM8 is addressable, allowing greater up-dating of information at a faster rate. The channel selection of the MM8 is accomplished by using

a Programmer Sequencer, such as the SCL-1. Output from the multiplexer is fed to a moderate speed sample-and-hold circuit, such as the SHM-1. The output of the sample-and-hold circuit is fed to a high performance A/D converter. The three mentioned units can be grouped on a single board, and the 13 bit BCD data fed to a Demultiplexing board where the signals are fed to respective display latches and display decoders. The conversion time per channel is approximately 15 microseconds. Assuming all eight channels were used, each channel is updated every 128 microseconds. Slower update times, or select only upon command is also available by altering the commands to the Programmer Sequencer.

Assuming the BCD data is available to a set of latches, the next problem is to redesign the SWR calculator.

The SWR calculation should be a function only of the forward power and reflected power indications, and independent of any critical parts or power supply variations. The use of a standard calculator chip with memory accomplishes all of the desire objectives. Figure (30) shows a proposed circuit utilizing a calculator chip. To operate the calculator chip, a hardwired program card is required. Figures (31) and (32) show the constructed programmer cards. The program sequence for operation of the calculator chip is listed as follows:

<u>Pulse Code</u>	<u>Function</u>	<u>Comments</u>
00000	enable "clear"	Clears system
00001	enter MSB_r	most sign. bit
00010	enter $2SB_r$	
00011	enter LSB_r	
00100	enable "enter"	Reflected Power number in reg.

<u>Pulse Code</u>	<u>Function</u>	<u>Comments</u>
00101	enter MSB_f	
00110	enter $2SB_f$	
00111	enter LSB_f	Forward Power number entered
01000	enable " \div "	P_r/P_f
01001	enable "sq. root"	
01010	enable "memory"	
01011	enable "1"	enter number "1"
01100	recall memory	
01101	enable "add"	
01110	enable "1"	enter number "1"
01111	recall memory	
10000	enable " - "	
10001	enable " "	
10010	enable display	SWR Displayed
10011	reset counter to 00000	

This microporgram computes the SWR from the displayed values of forward power and reflected power. The program written assumes the calculator chip has a memory and an operating register. If only a memory is availble a variation of the program can be written. The use of the calculator chip eleiminates the inaccuracies inherent in the analog calculator. The output of the calculator chip can be fed to a set of lathces, and to the SWR Alarm Board. Once entered in the SWR Alarm Board, the alarm sequence is as described in the thesis text. The projected cost of the recommended modifications is \$875.00. If the above

recommendations were incorporated into a second generation model, the total construction cost would be approximately \$1,200.00 total procurement cost.

If an accurate SWR is realizable, it is possible, by using several additional bits of information, to determine the input impedance of an antenna under test. In order to determine the input impedance of an antenna, SWR, phase angle between the forward and reflected voltages, and the length of the line in wavelengths must be known. The SWR can be determined by either of the methods discussed. The length of the transmission line is either known, or determined by time-domain reflectometry. By utilizing the frequency readout the length of the line in wavelengths at the operating frequency can be computed.

$$L_{\lambda}(\text{ft}) = \frac{9.6 \times 10^2}{f(\text{MHz})\sqrt{\epsilon_r\mu_r}} \quad (8)$$

An additional circuit is required to determine the phase angle between the forward and the reflected wave. Figure (33) shows a block diagram of a circuit to measure the phase angle between the forward and reflected wave. Once these three items have been determined, the input impedance of the antenna of interest can be determined as follows. The SWR indicated on the panel face is used as the radius of a circle. The circle, with the SWR as a radius is drawn with the origin at 1 on a Smith Chart, figure (34). The value of the phase angle is located on the edge of the Smith Chart and marked. A straight line is drawn from the center of the SWR circle, 1 on the graph, to the value of the phase angle as marked on the edge of the Smith Chart. The intersection of the SWR circle and the drawn line indicates the impedance at the point of the

sensor. If the sensor is located at the transmitter, the value of impedance is the impedance as seen by the transmitter at the operating frequency. To determine the value of the antenna terminal impedance, start from the intersection of the SWR circle and the straight line and rotate around the SWR circle on the Smith Chart in a counter-clockwise direction a distance L_λ as calculated in equation (8), and mark the termination point. The mark is then read as a real and a reactive value. This value represents the value of the antenna terminal impedance when multiplied by the characteristic impedance of the transmission line.

As an example, assume an operating frequency indication of 7.250 MHz, a SWR of 1.75:1, an indicated phase angle of 140 degrees, and a transmission line length of 88 feet. From equation (8) the length of the transmission line in wavelengths is 1.78. Draw a circle with radius 1.75 at origin 1 on the Smith Chart. Locate 140 degrees on the outer edge of the chart, draw a straight line to the center of the SWR circle from the 140° mark on the edge of the Smith Chart. The intersection of the straight line and the SWR circle occurs at $0.62 + j0.25$. Multiplying this figure by the characteristic impedance (assuming 50 ohms), the impedance is $31 + j12.5$ ohms. This is the impedance as seen by the transmitter. Moving in a counterclockwise direction around the SWR circle for a distance of 1.78 wavelengths, the impedance at the antenna terminals is $50(1.65 - j0.30)$ or $82.5 - j15.0$ ohms.

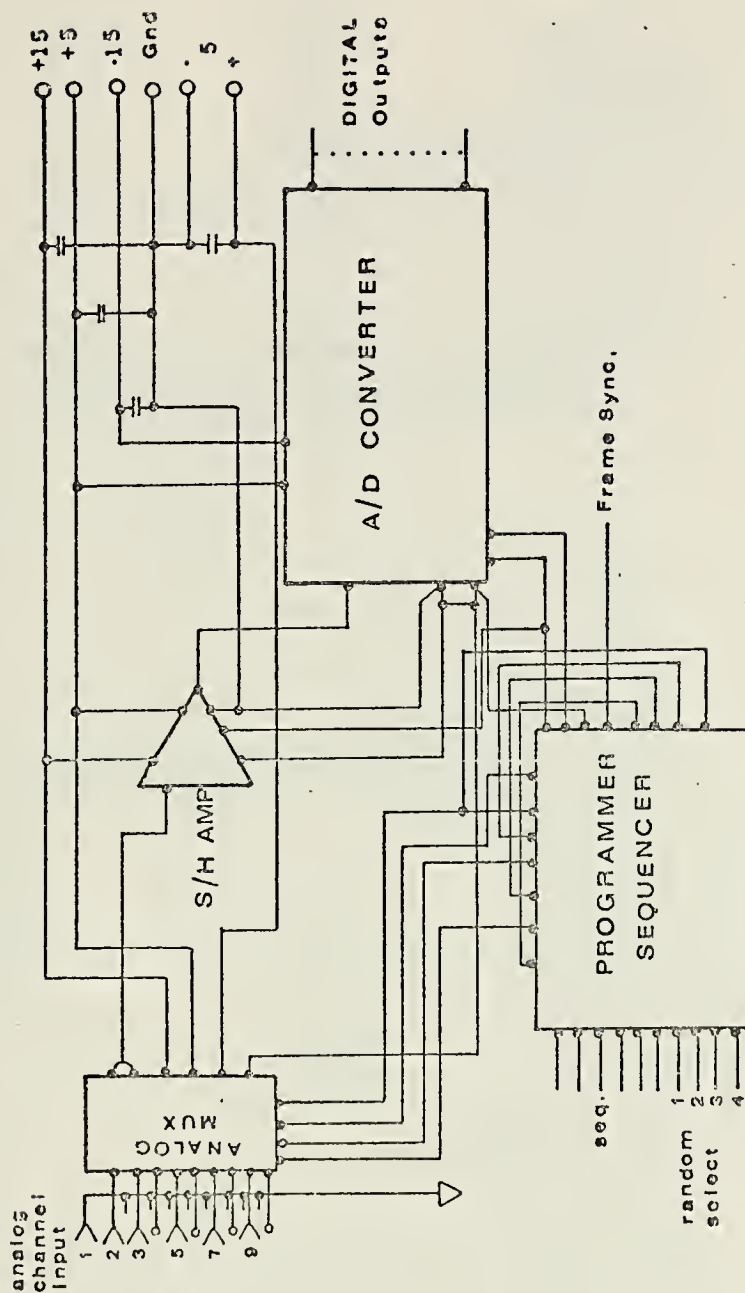
From the example, if the antenna had a design terminal impedance of 50 ohms, even though it is fed from coaxial cable with a characteristic impedance of 50 ohms, the impedance at the end of the cable, as seen by the antenna is 83.8 ohms at an angle of -12.6 degrees. This is nearly 70% greater than the desired termination impedance.

The terminal impedance as determined above, can be used to "chart" the antenna's terminal impedance at specified frequencies over a given period of time. These impedance charts can then be used to predict impending failures or problems before they become so severe as to cause failure.

Properly used, the information should enable greater energy to be transferred from the transmitter to the antenna, less loss due to reactive dissipation, and increased mean-life of the transmitters.

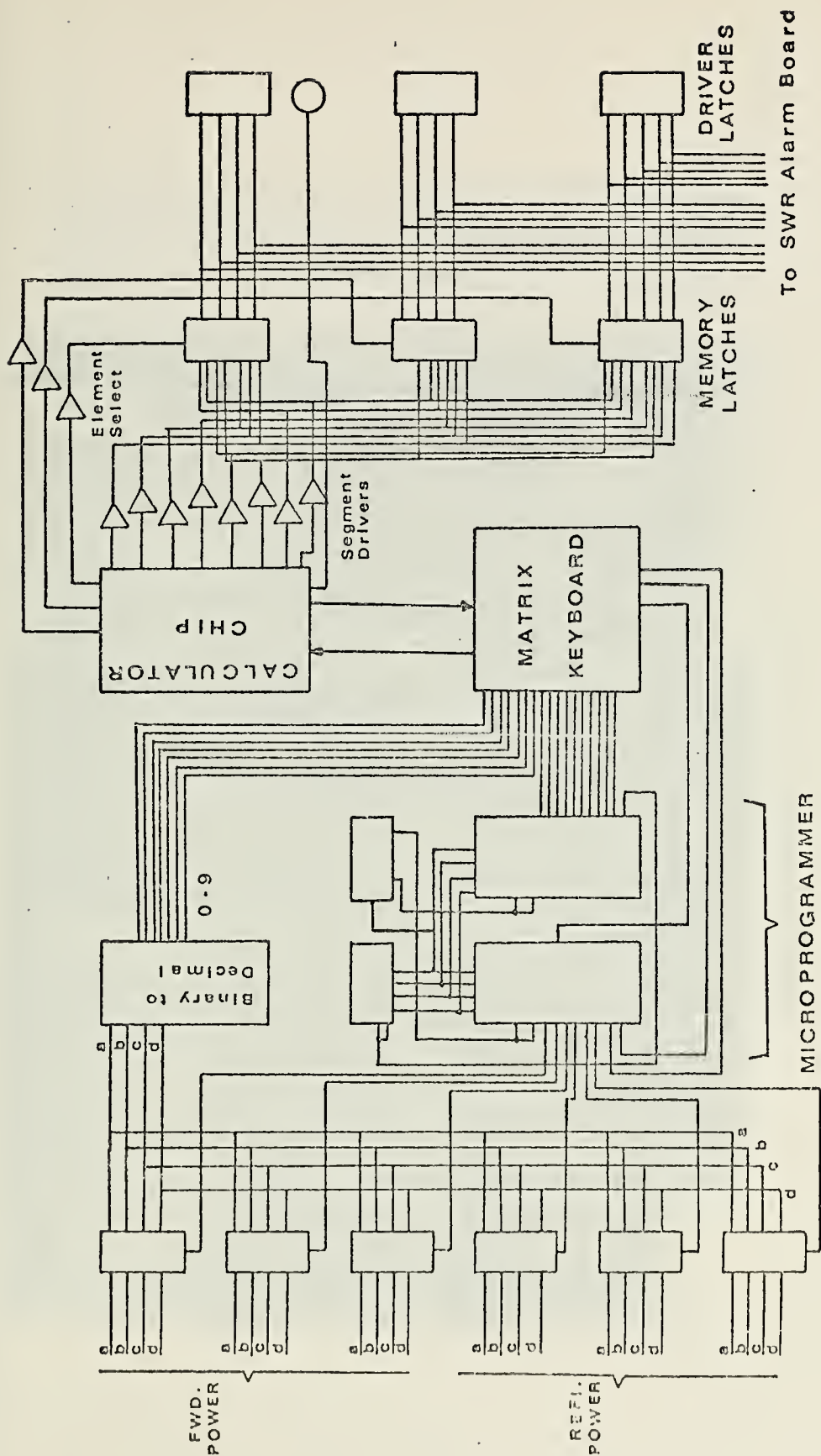
The prototype unit constructed used wire runs to connect the vector sockets together. A total of 700 separate wire connections were made. Future prototypes should include a "mother-board" on which is etched the wire runs. This would decrease the construction time considerable, as well as increase the usable working size of the boards.

The recommendations made should increase the efficiency, dependability, and usability of the systems analyzer.



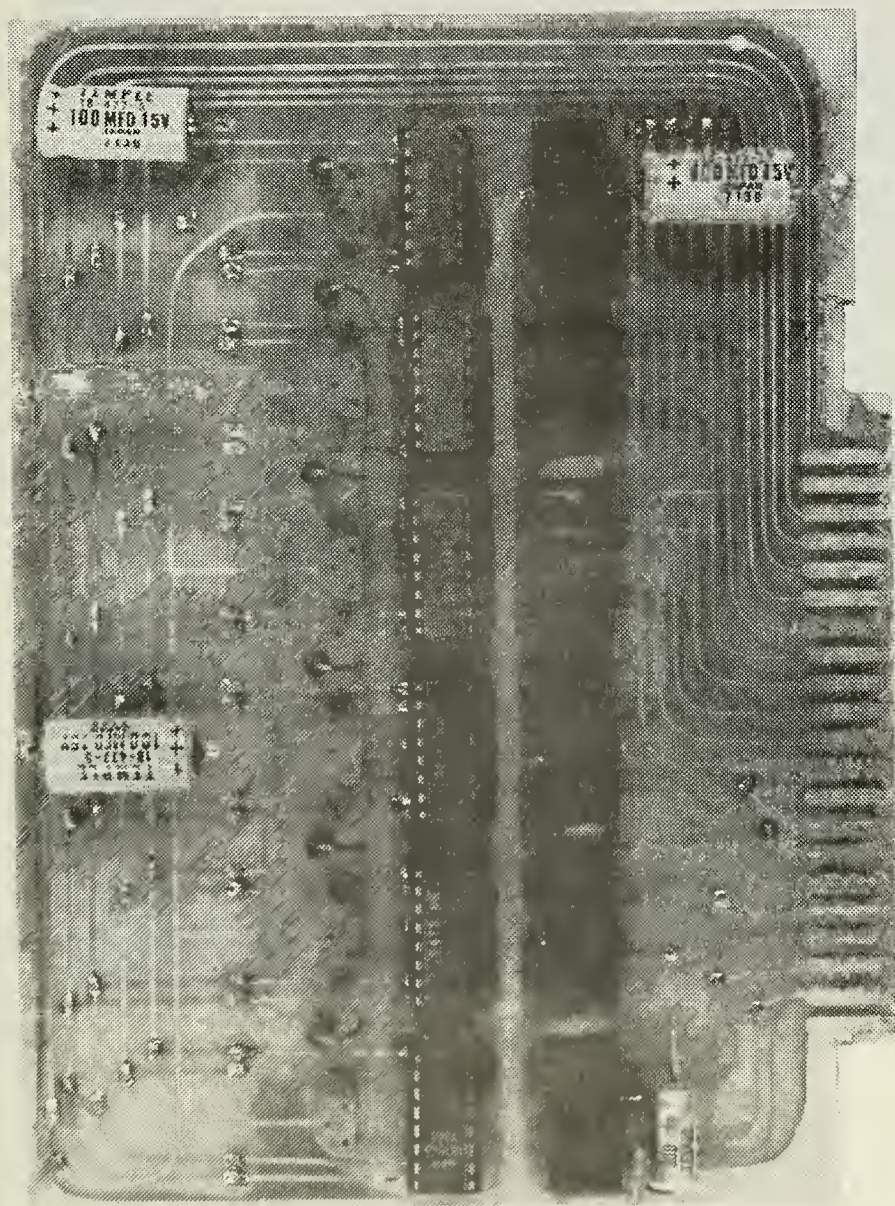
ANALOG MULTIPLEXER
AND DIGITAL CONVERTER

Figure (29)



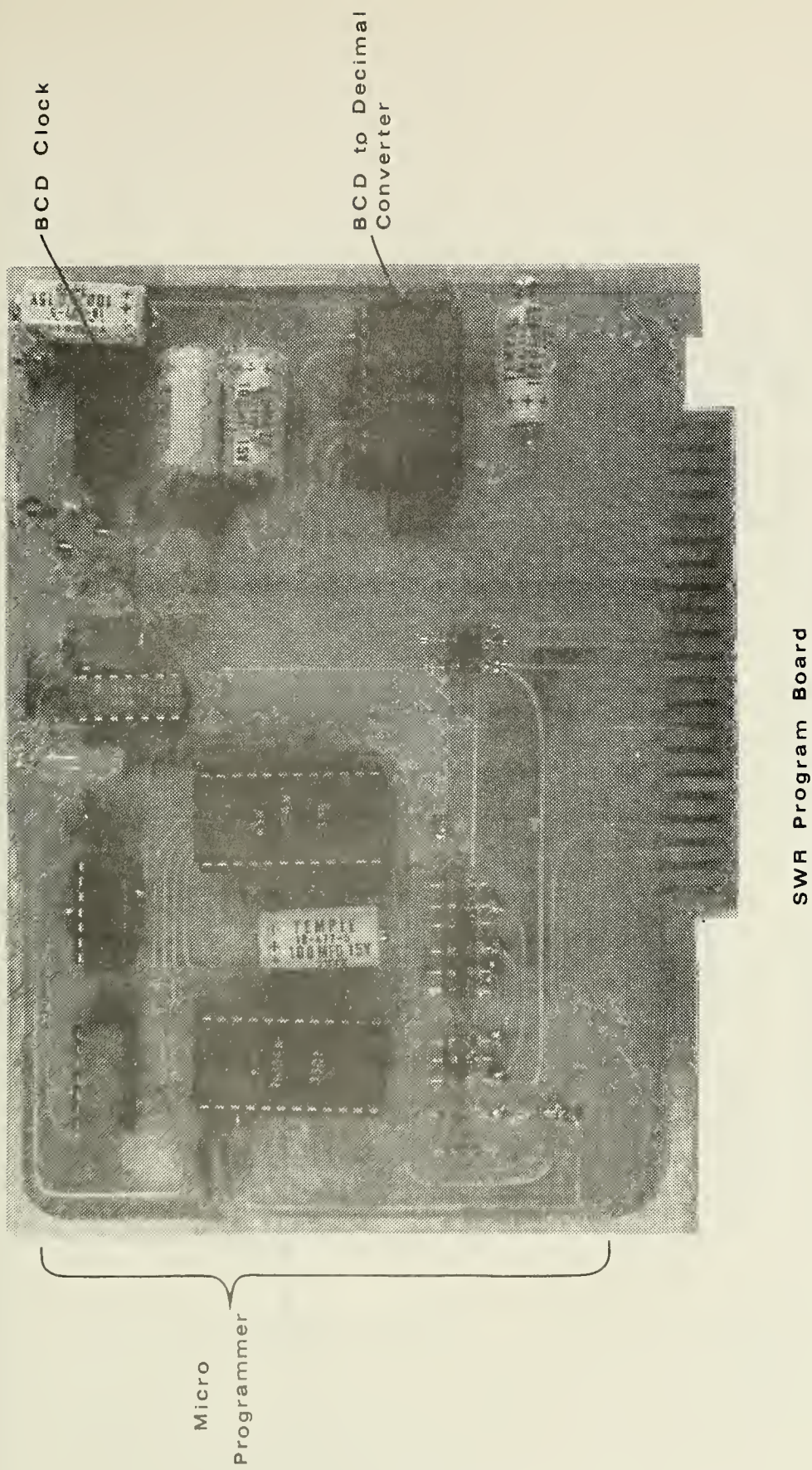
SWR DIGITAL CALCULATOR

Figure (30)



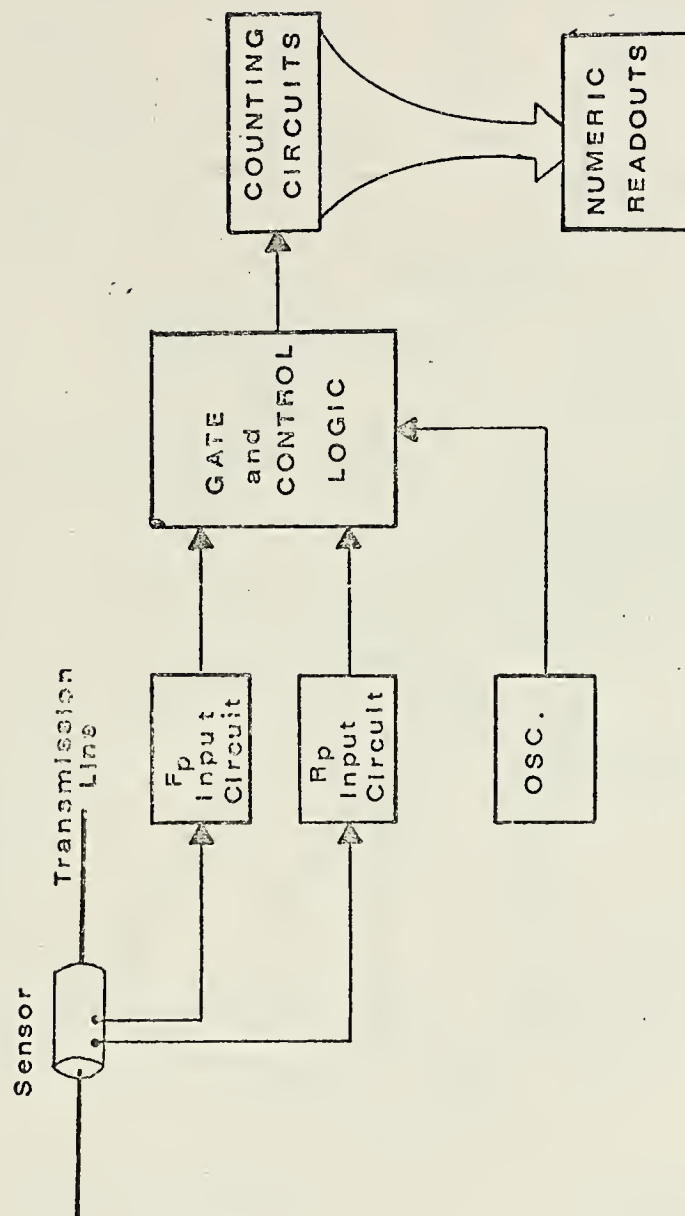
SWR BCD Multiplex Input/Output

FIGURE 31



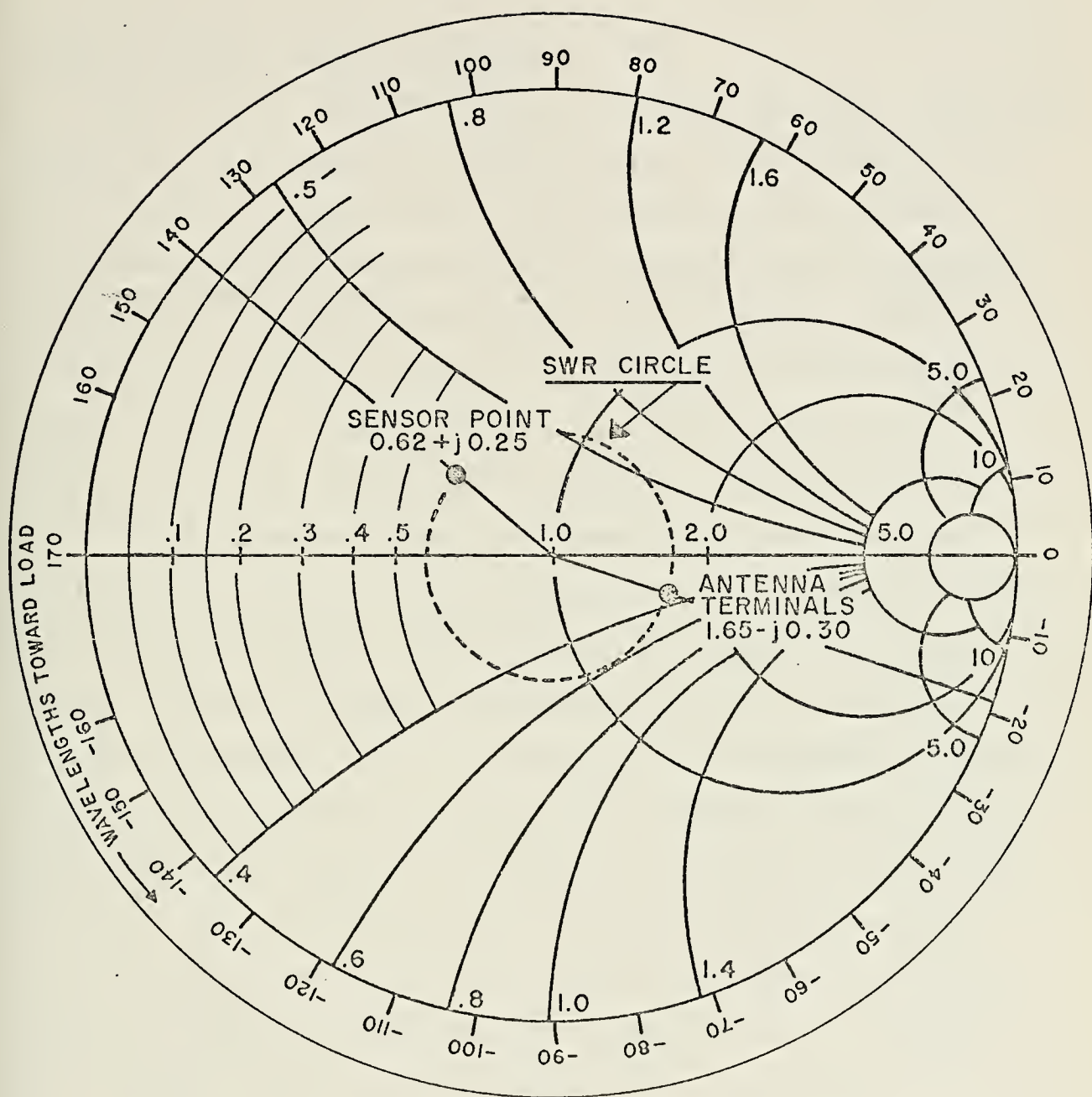
SWR Program Board

FIGURE 32



PHASE ANGLE DETECTOR

Figure (33)



SMITH CHART

$f = 7.25 \text{ MHz}$

$\text{SWR} = 1.75$

$\angle = +140^\circ$

FIGURE (34)

APPENDIX A

DETAILED FREQUENCY COUNTER OPERATION

Figure (35) is a schematic diagram of the frequency counter. Referring to figure (35), a frequency is applied to input "C" via connector "A" or "B". Capacitor C_1 removes a d.c. which might be present on the line. C_2 prevents excessive attenuation of high frequency signals and resistor R_2 and diodes D_1 , D_2 prevent overloading of the input to Q_1 . Input transistors Q_1 and Q_2 form a direct coupled amplifier circuit with 100% negative feedback. Q_1 and Q_2 provide wide bandwidth, high input impedance, low output impedance, and a unity gain. The signal from Q_1 , Q_2 is direct coupled to the base of a common-emitter amplifier Q_3 . Q_3 amplifies the signal and is direct coupled to an isolation amplifier Q_4 . Q_4 provides the triggering signal to the Schmitt trigger circuit, Q_5 and Q_6 . The Schmitt trigger is a regenerative bistable circuit which produces a square-wave output. Q_5 and Q_6 are emitter-coupled for current-mode operation of the first decade counter. Input sensitivity controls R_C and R_F adjust the threshold of the Schmitt trigger circuit to insure that very small signals can be measured. The output of the Schmitt trigger circuit is coupled to the emitter follower Q_7 . Q_7 keeps the transistor-transistor logic from loading the Schmitt trigger circuit. The output of Q_7 (either "0" or +5 volts) is applied to the clock-input of IC-1. IC-1, 2, 3, and 4 are connected as an asynchronous BCD counter. Each of the flip-flops are triggered by negative-going pulses. Flip-flop IC-1 is toggled by the signal from Q_7 . As IC-2 is toggled on every input pulse when both the J and K inputs are at logic "1", the Q output goes to a logic "1" on the 1st, 3rd, 5th, 7th, and 9th counts.

These pulses are applied to the toggle input of IC-2. Because of the feedback loop from \overline{Q} of IC-4 to the J input of IC-2, IC-2 is inhibited on the tenth count. This results in the Q output of IC-2 being a logic "1" for the 2nd, 3rd, 6th, and 7th counts. IC-3 is toggled by the Q output of IC-2 on the 4th and 8th counts. Thus the output of IC-3 is a logic "1" for the 4th, 5th, 6th, and 7th counts.

Reset is accomplished by taking all clear inputs of the flip-flops to a logic "0". These logic levels are supplied by IC-29(D). Counting is started when the J and K inputs of IC-1 are returned to logic "1", and inhibited when these inputs are returned to logic "0". The Control logic for the J and K terminals of IC-1 are taken from either IC-25 or IC-28 dependent upon the position of the range switch.

The outputs of IC-1,2,3, and 4 are fed to a memory latch IC-13. The overflow of IC-4 is fed to IC-5, a decade counter. IC-5,6,7, and 8 are decade counters activated by the overflow of the preceeding decade counter. The output of each counter is fed directly to a memory latch IC-8,9,10,11,12, and 13. When the control signal to the latches is at a logic "1" information present at the input terminals of the latches is transferred to the readout.

The information from the memory latches is decoded by IC-30,31,32,33,34, and 35. From the decoders the information is fed to the display LEDs. Table (5) shows how the information is decoded.

BINARY				DECIMAL
A	B	C	D	
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9

TABLE 5

If a code other than BCD is received by the driver the display will not register valid information. This condition can only occur when the counter is first turned on, or when the range switch is changed with a frequency input applied. If this does occur, the next reset and transfer pulse will remove the false code and the subsequent display will be valid.

1 MHz CLOCK AND SCALERS

A 1 MHz crystal and two sections of a quad-two NAND gate are used to form a transistor-transistor logic compatible clock. Capacitor C_{11} is an air-tuned variable used to calibrate the oscillator to 1.00000 MHz. Section "b" of the quad-two NAND (IC-21) is used as a buffer to isolate

the oscillator from the first decade divider of the time base scaler.

The scaler section consists of six decade dividers. The range switch selects the output from the third or sixth divider for the reset pulse, and either the "A" output of IC-25 or the "Q" output of IC-28 for the input gating pulse. Therefore the range switch can provide either a 1-millisecond (for MHz operation) or a 1-second (for KHz operation) time base for the gating, reset, and memory circuits. The "A" output of IC-27 provides the transfer pulse.

GATING, MEMORY, AND RESET CIRCUITS

The gating, memory, and reset circuit controls the times that an input signal is gated into the counting circuits, and the times the digital information is passed from the counting circuits to the display LEDs. Figure (36) shows the timing relationships of the gating, memory, and reset circuit.

When the range switch is in the MHz position, the "gate open" signal is a 1-millisecond pulse obtained from the output of IC-25 (pin 12). The input signal enters the counters during the millisecond that the logic "1" of the gating signal is present on the J and K inputs of the first flip-flop of the first decade divider (pins 9 and 3 of IC-1).

The reset pulse is derived by combining the inverted gate signal with the output of IC-24 in IC-29(d). During the time that both the output of IC-24 and the inverted gate signal from IC-29(c) are high, a logic "1" at both inputs of the NAND gate IC-29(d) causes a logic "0" reset pulse to be applied to the first decade counting unit and to IC-20 (pin 6), the overrange flip-flop. This reset pulse is inverted by Q_8 to supply a logic "1" reset pulse to IC-5,6,7, and 8.

The transfer signal is derived by combining the reset pulse with the inverted gate pulse in the NAND gate IC-29(a). The resulting pulse is inverted by IC-21(c). A transfer pulse cannot occur during a reset pulse because IC-29(b) is inhibited by a logic "0" on pin 4 from IC-21(c). The transfer pulse can occur only when pin 4 is at a logic "1" and during a positive-going transistion at pin 12 of IC-27.

When the range switch is in the KHz position, the gate open signal is a 1-second pulse that is obtained from the Q output (pin 12) of IC-20. All other operations are the same with the exception of the basic signals are obtained from the output (pin 11) of IC-27 and the \bar{Q} output of IC-20(a).

OVERRANGE INDICATION

Figure (37) shows the pulse relationships of the overrange detector. If the count passes from 99999 to 100000, a pulse is produced at the output (pin 11) of IC-8. This output triggers IC-20(b). The input of IC-20(b) is tied to logic "0", which caused the \bar{Q} output to latch in a logic "0" condition whenever the clock-input is triggered. The \bar{Q} output remains in this condition until a logic "0" is applied to the clear input. IC-19 is a quad-two NAND gate used as an inverting data latch. The logic level at pin 1 of IC-19 is inverted and transferred to pin 8 when pin 2 and pin 13 are both at logic "1". A logic "0" at these inputs will inhibit transfer. The output of the latch is connected to the base of a NPN transistor Q-10. The overrange lamp will light only when there is a logic "1" from pin 8 of IC-19. Figure (38) shows the integrated circuit base diagrams. Figure (59) shows the completed frequency counter printed circuit board.

circuits constructed and checked on the test board generally worked when hard-wired on a card. In order to check the constructed cards a 22 double pin and a 18 double pin socket were located on the apron of the test board and hard-wired into the test strip adjacent to them. Boards could thus be pulled from the mainframe and placed in the socket. Pin connections were made by connections to the adjacent test strip. Once wired, any desired test could be performed.

The use of the digital test board resulted in better circuit production since a wide variety of logic inputs were easily available. For any type of digital work, a test board of some type is a necessity. In digital work, more than "just" a test board is required. Dedicated power supplies, clocks, indicators, readouts, etc., are no longer a luxury, but an absolute necessity.

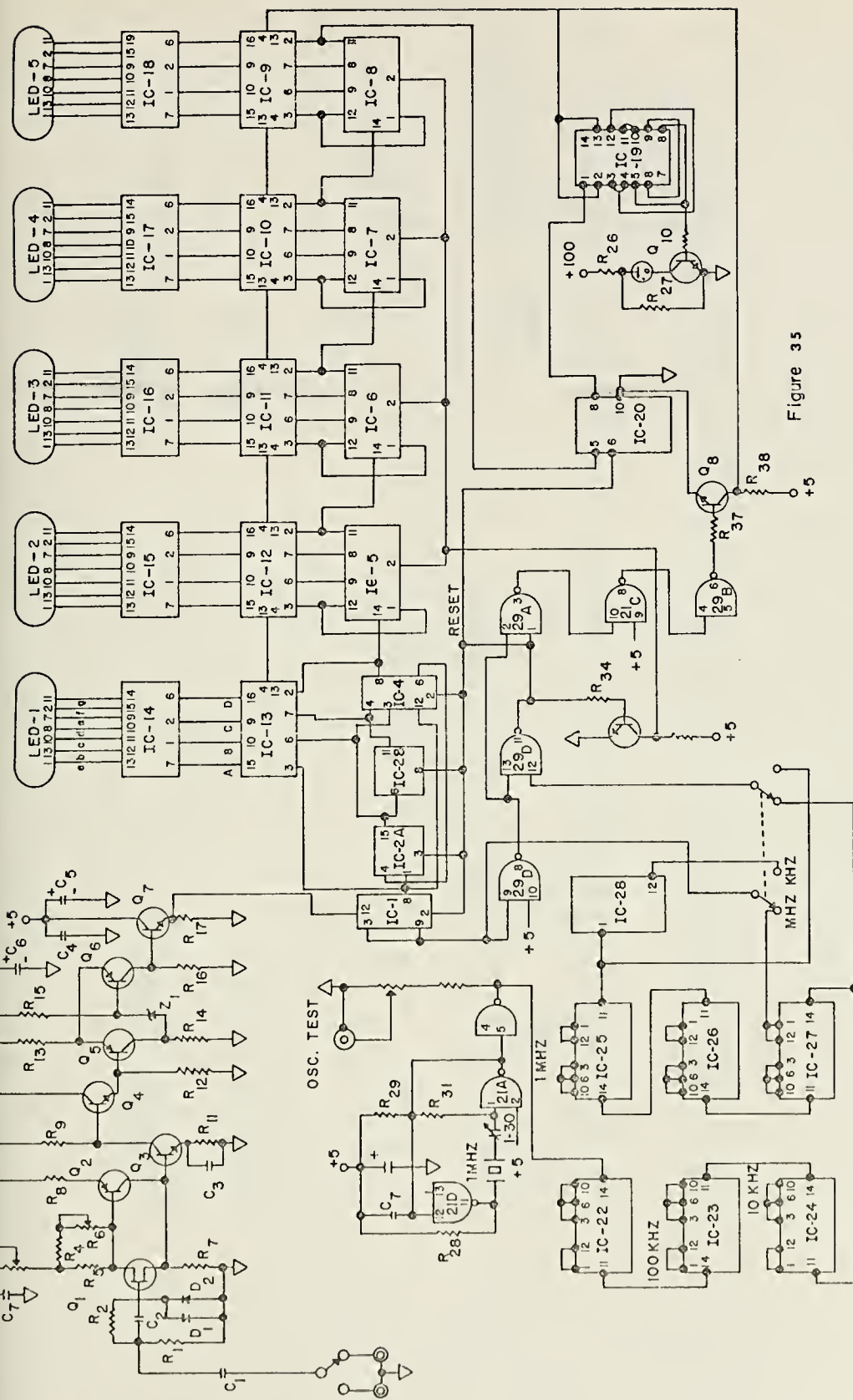
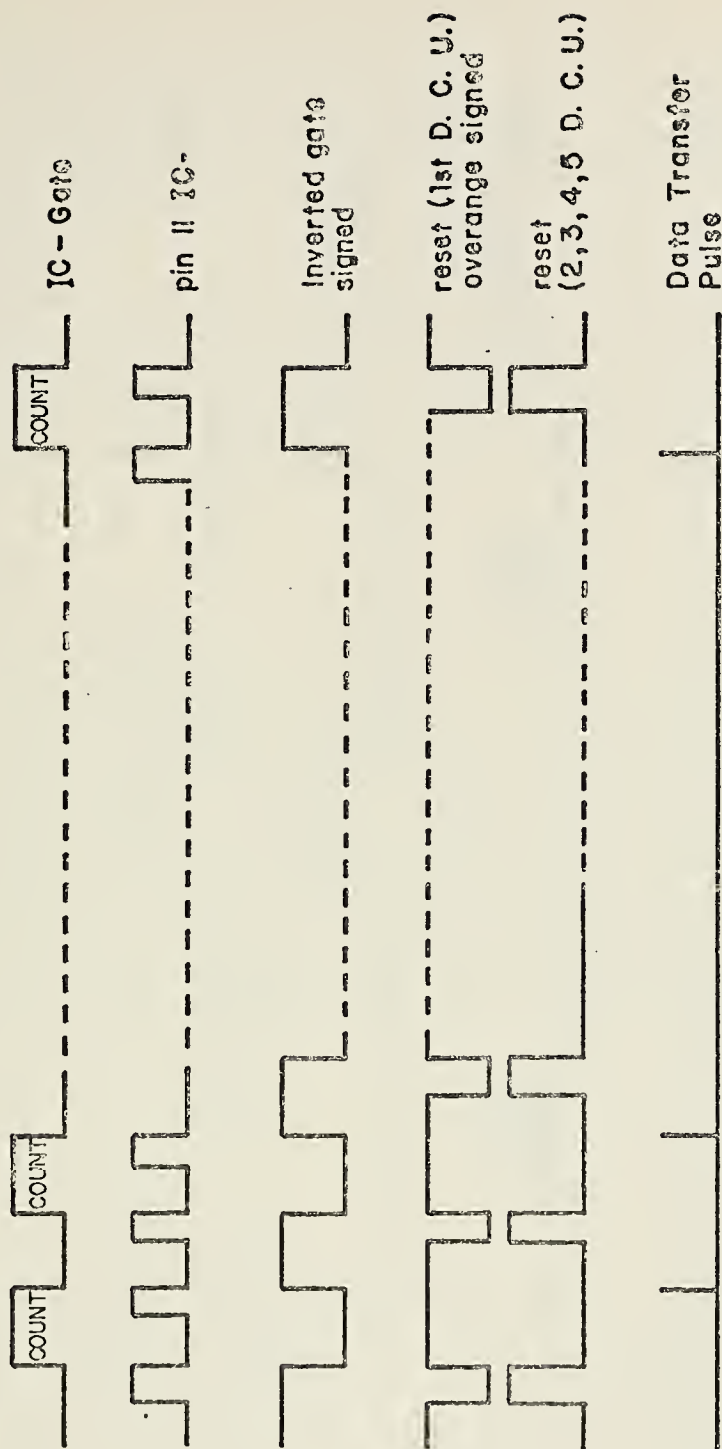
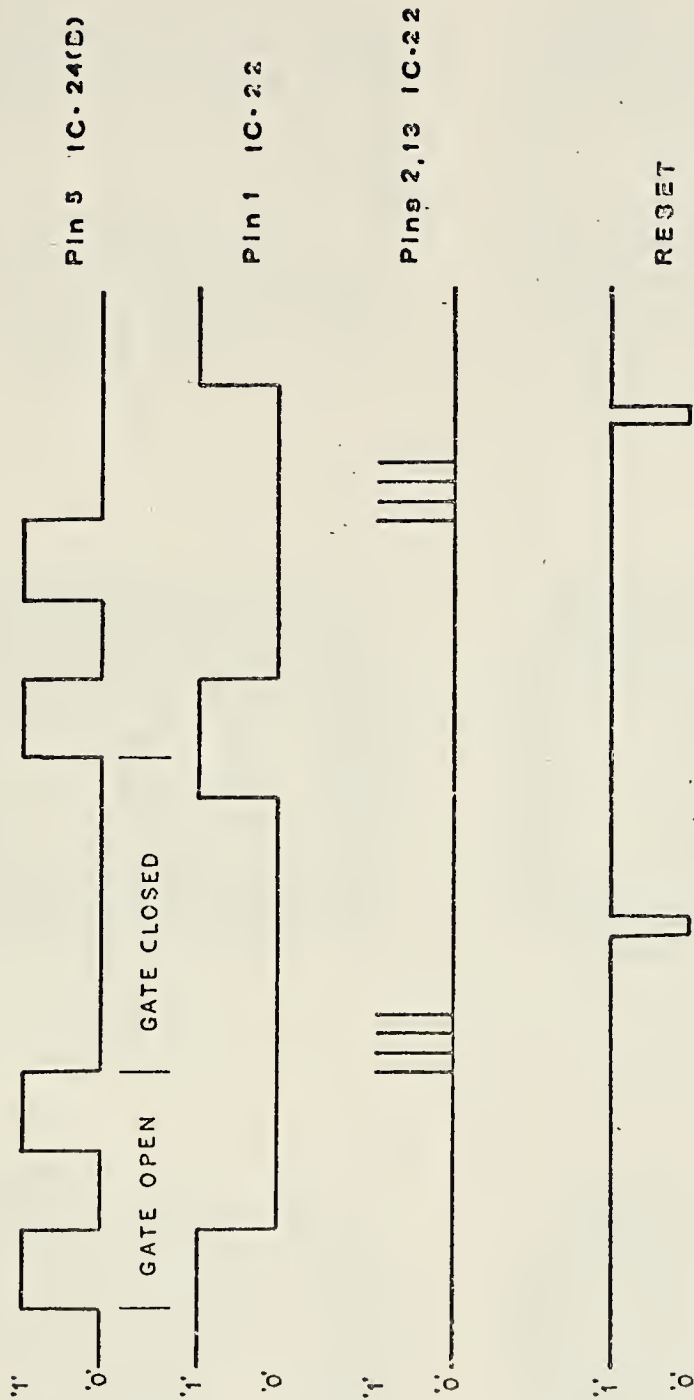


Figure 35



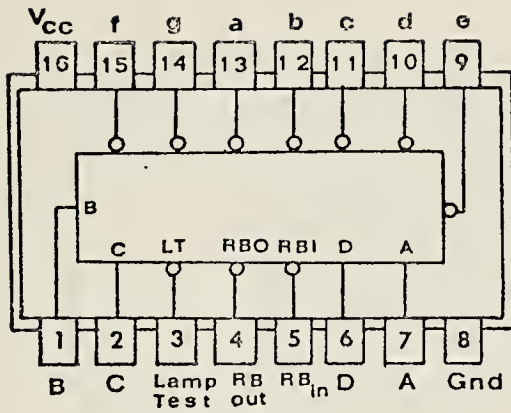
Timing Relationships

Figure (36)

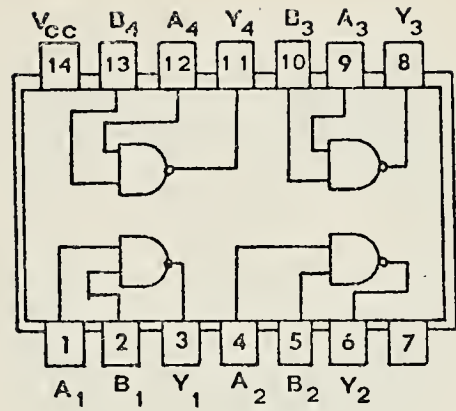


OVERRRANGE DETECTOR
PULSE RELATIONSHIP

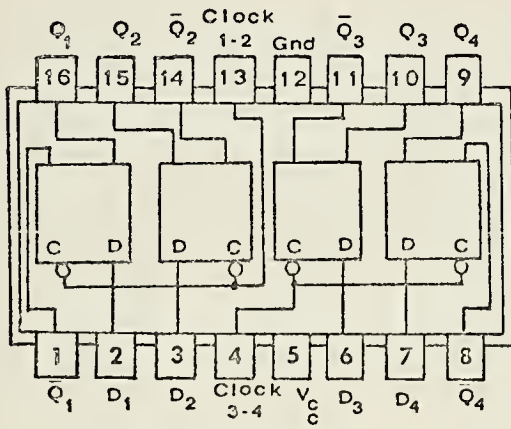
Figure (37)



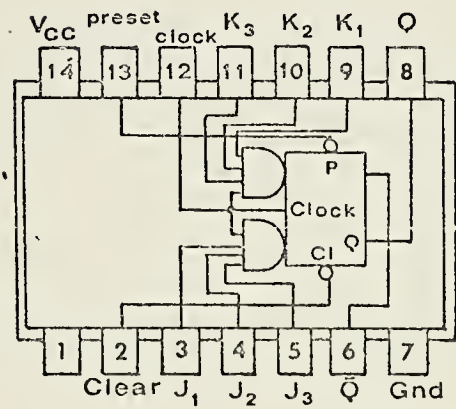
7447



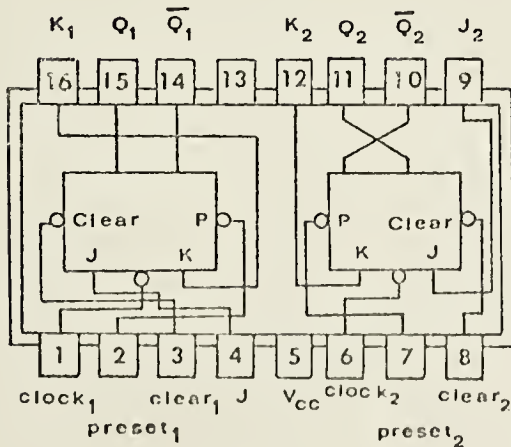
7400



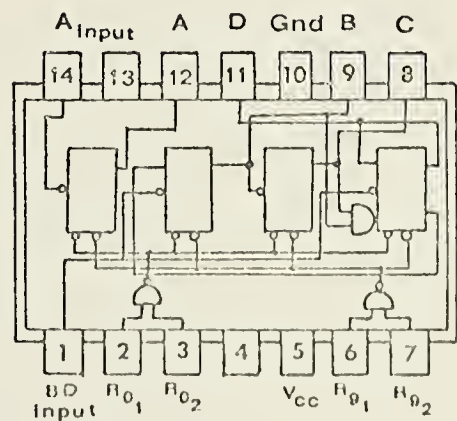
7475



7472



7476

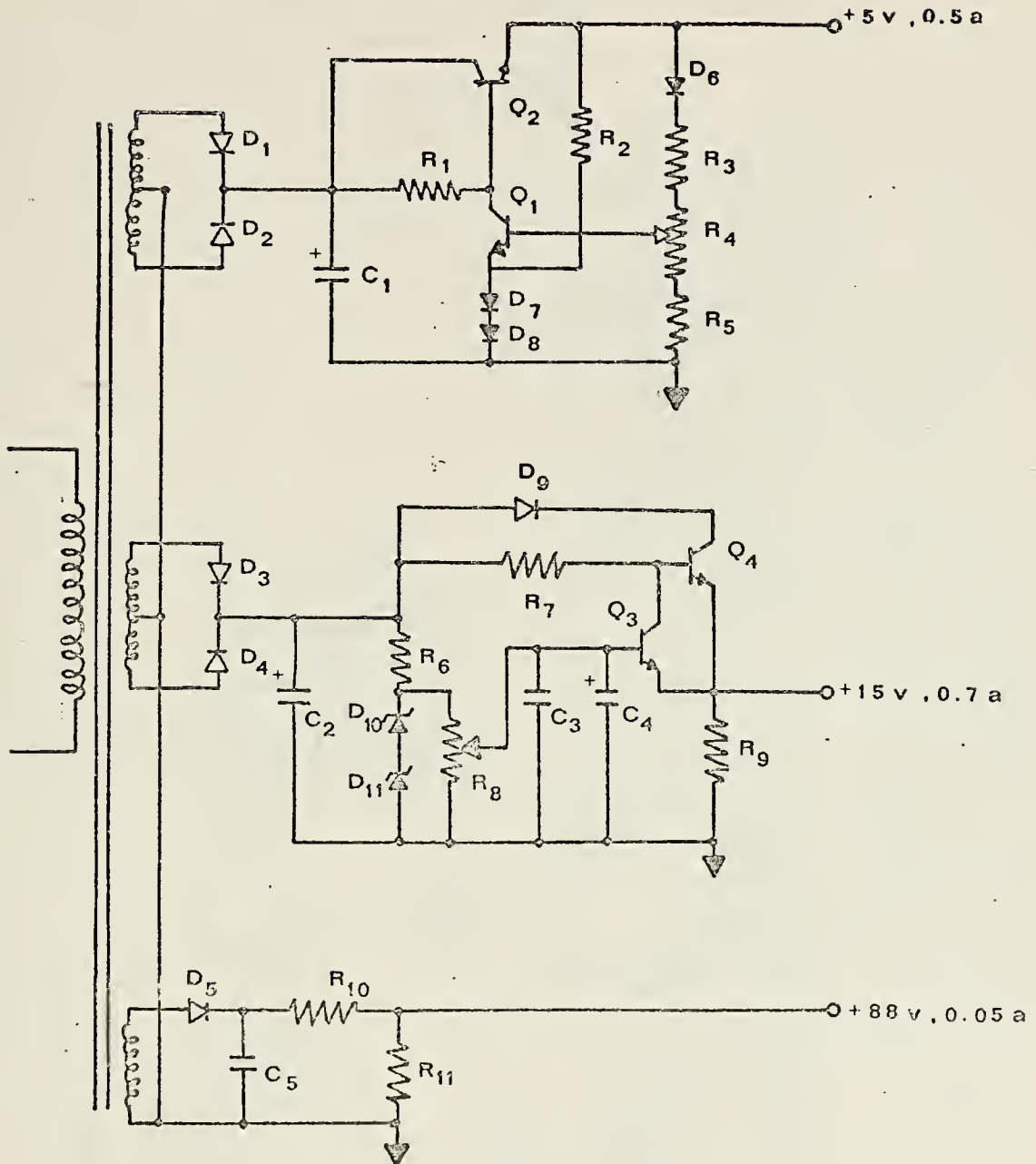


7490

Figure (38)

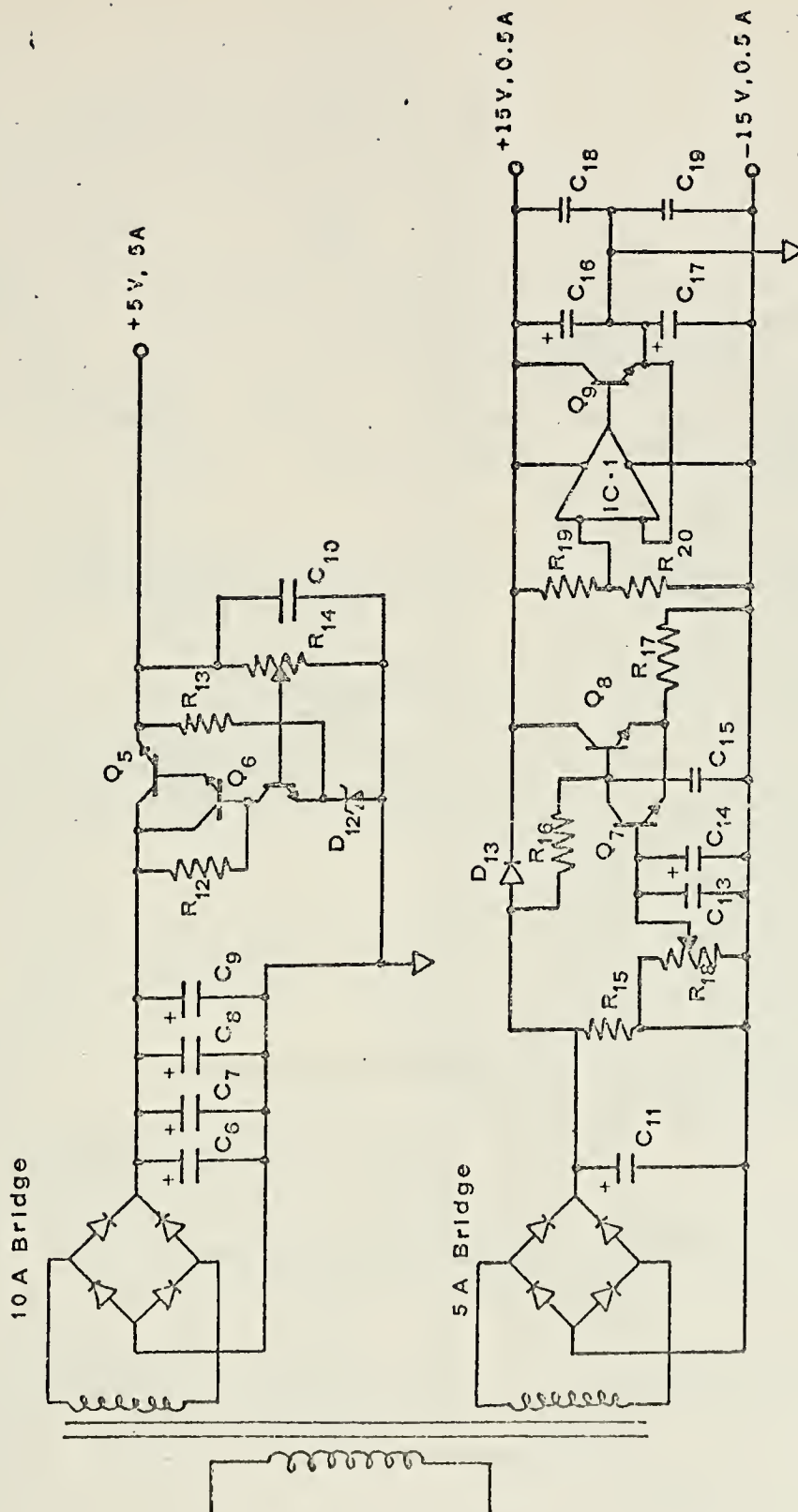
APPENDIX B

POWER SUPPLY AND MAIN FRAME WIRING DIAGRAMS



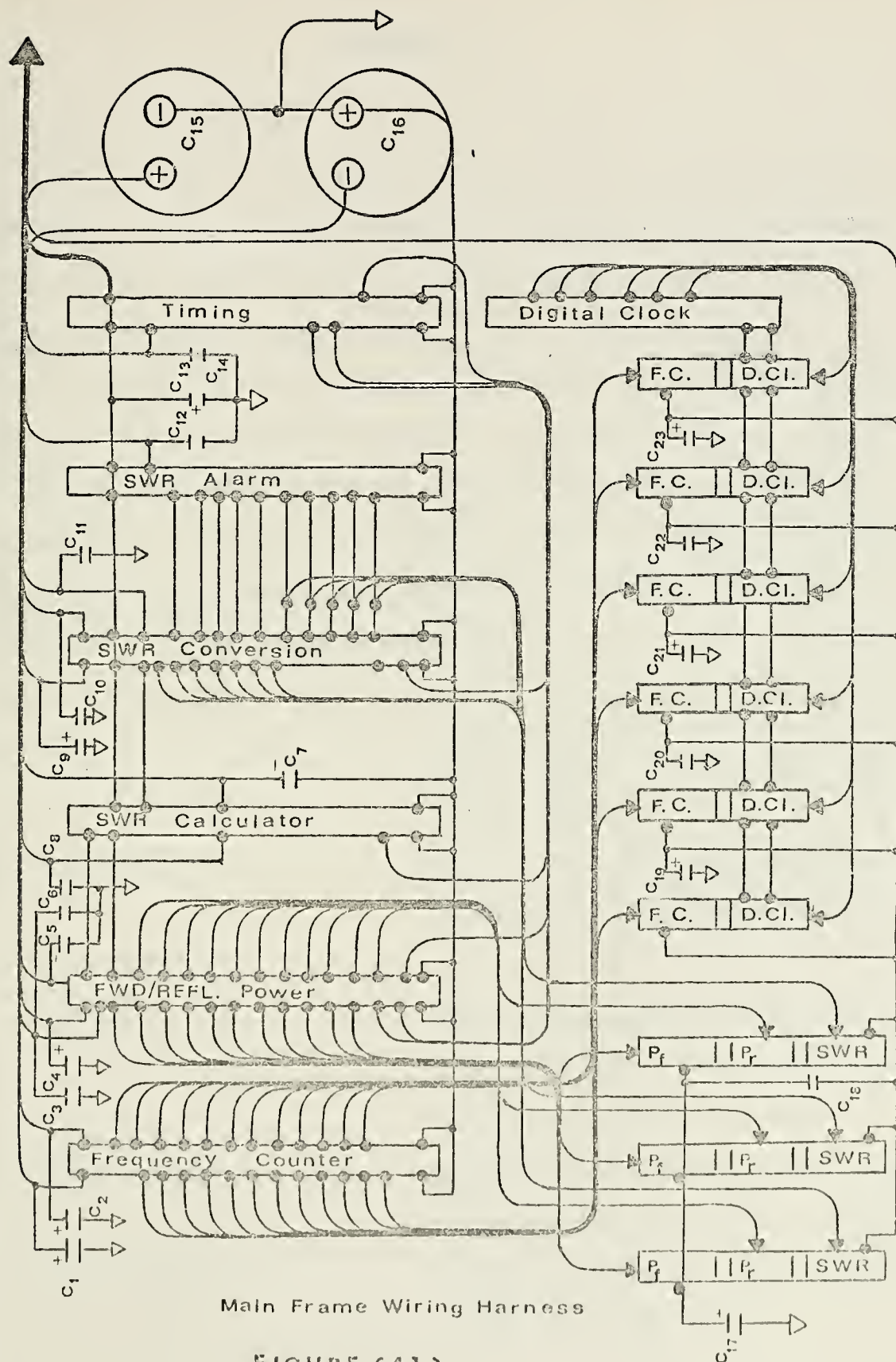
FREQUENCY COUNTER POWER SUPPLY

Figure (39)



5 Volt, ± 15 VOLT POWER SUPPLY

Figure (40)



Main Frame Wiring Harness

FIGURE (41)

APPENDIX C

1. DIGITAL TEST EQUIPMENT

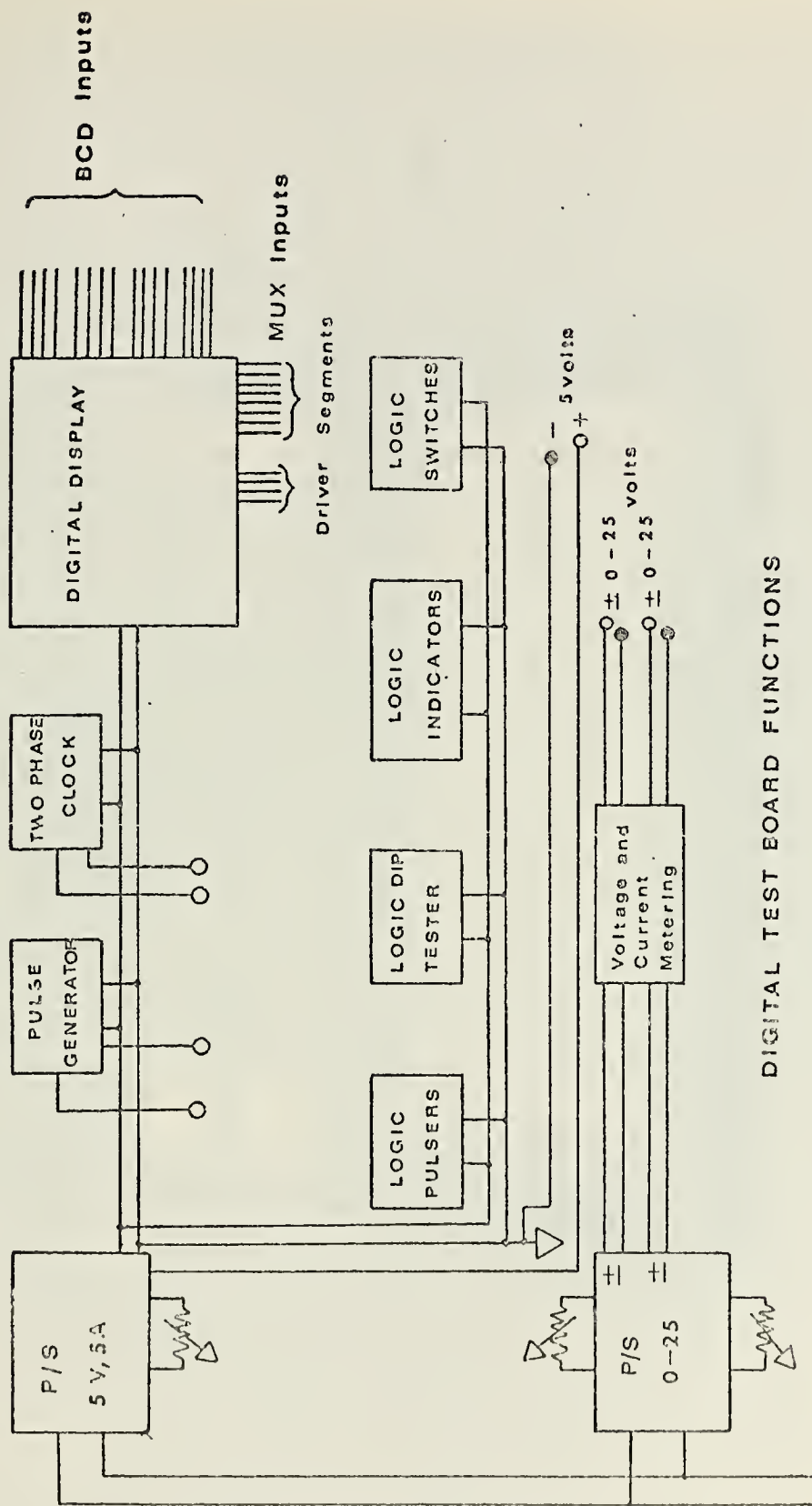
Testing of designed circuits utilizing TTL/DTL logic was initially difficult due to lack of bread-boarding equipment, sufficient dedicated power supplies, and the need for auxiliary equipment such as clocks, counters, and logic state-indicators. After several attempts to evaluate design circuits by hard-wire techniques, it was decided to stop construction of the analyzer mainframe and to design and build a digital breadboard. The decision to build was primarily based on need and cost. A commercially built digital breadboard, such as the Electronics Instrument digital design board, costs in excess of \$ 500.00. The design requirements for the digital breadboard are:

1. Variable ClockTwo square wave outputs 180° out of phase, logic "1" output. Range from 1 Hz to 100 KHz.
2. Power SuppliesTwo 0-15 volt, floating ground supplies with output voltage and current metering.
3. Variable Pulse GeneratorSingle pulse output for any negative going input wave. Pulse width variable from 1 microsecond to 4 seconds.
4. Manual PulsersManually activated clock pulses. One pulse each time the switch is depressed.
5. Logic SwitchesSwitches which set the output at either a logic "1" or logic "0".

6. Logic IndicatorsTen indicator lamps which illuminate when a logic "1" is entered. State indicators draw less than 20 microamps load current from test circuit.
7. Logic DIP TesterAllows a chip to be tested out of the circuit for state conditions and for proper operation. State or operation conditions indicated by red-LEDs. Logic "0" turns off the LED indicator.
8. BCD/MUX Digit IndicatorsFour numeric LEDs with decoders and face panel connections for BCD inputs. Four numeric LEDs wired for MUX operation with face panel connections for multiplexed digital data.
9. Tri-state Indicator.....Probe sensor for testing logic circuit logic level. Indicates logic "1", "0", or open. Draws less than 10 microamps from test circuit.

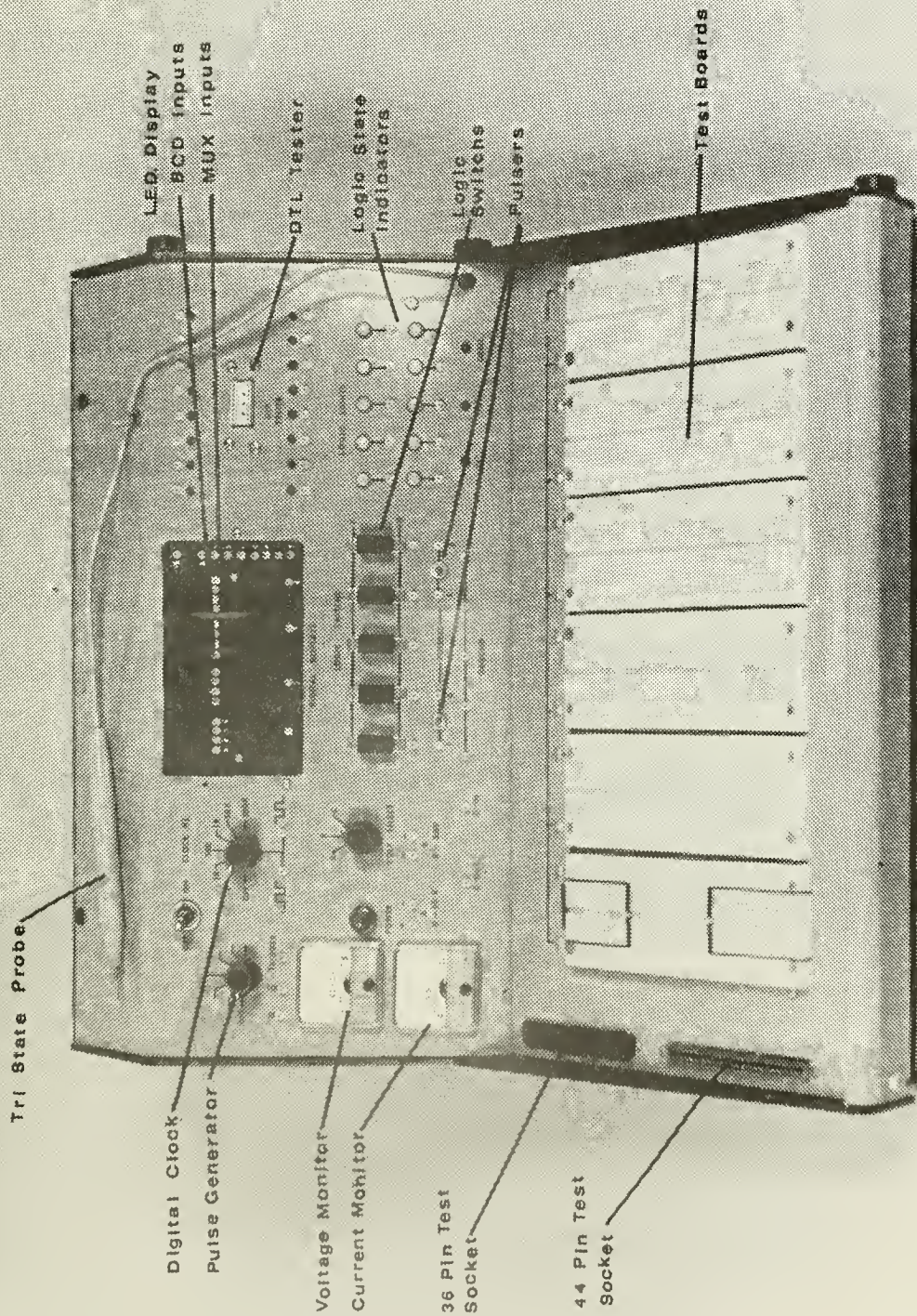
Figure (43) is a photo of the digital test board constructed. Figure (42) shows a block diagram of the test board functions. A detailed description of each circuit is not included. Construction of the circuit boards were as described in section III(B).

The digital test board, once completed, more than served its purpose. TTL, Hybrid, and DTL circuits were constructed on the breadboard and tested for operation. Since the necessary timing pulses were readily available, as were the logic state-indicators, power supplies, etc.,



DIGITAL TEST BOARD FUNCTIONS

FIGURE (42)



DTL TEST SET

FIGURE 43

APPENDIX D

PHOTOGRAPHIC VIEWS OF PROTOTYPE BOARDS AND EQUIPMENT

Various views of the completed prototype boards and quipement are included herein as an aid in understanding the details of fabrication and operation of the system.

The front panel view, figure (45) shows the readout locations, and all operating as well as indication devices. Location of indicating LEDs, operational switches, and antenna indicators is based on assumed operator usage.

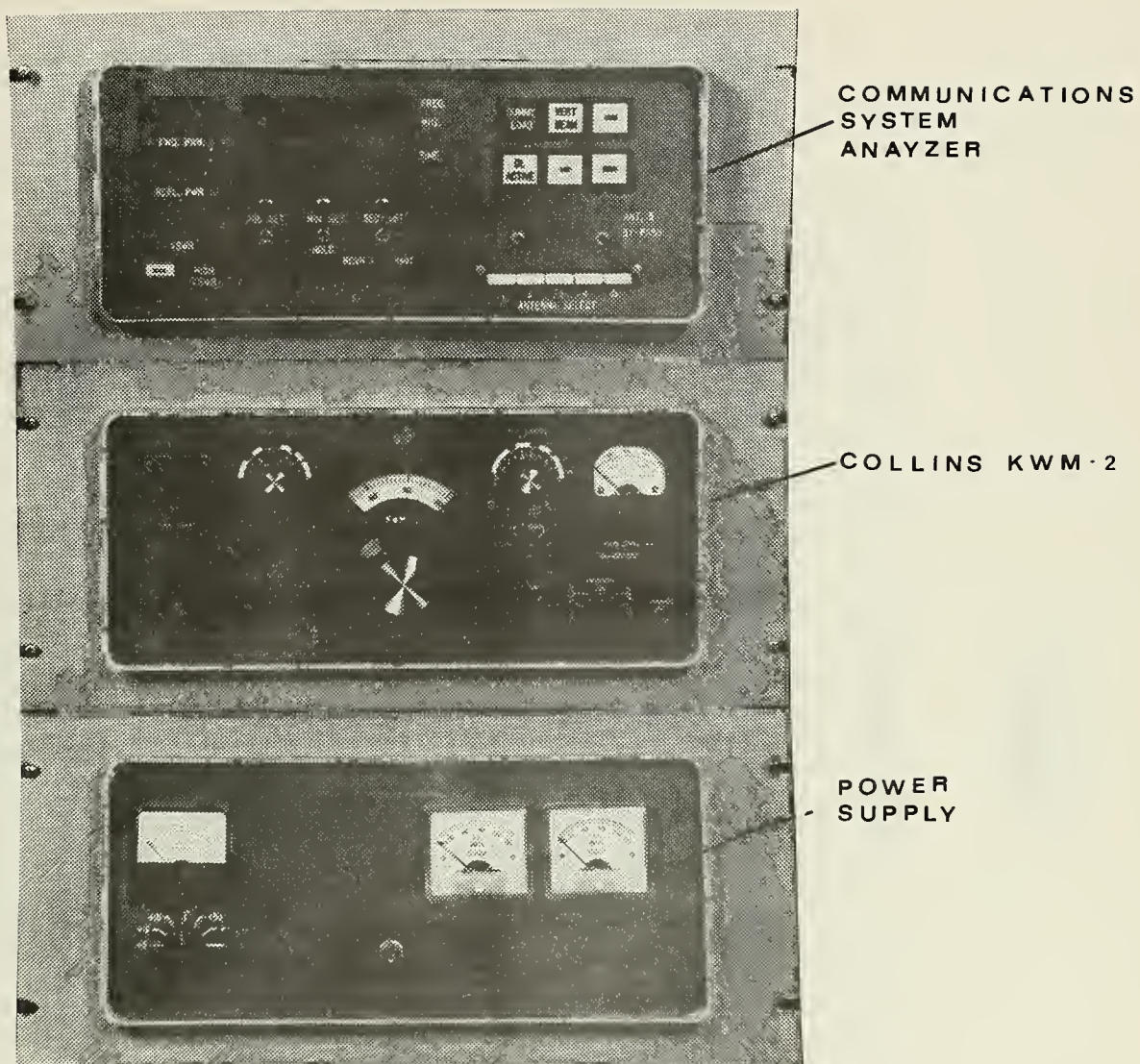
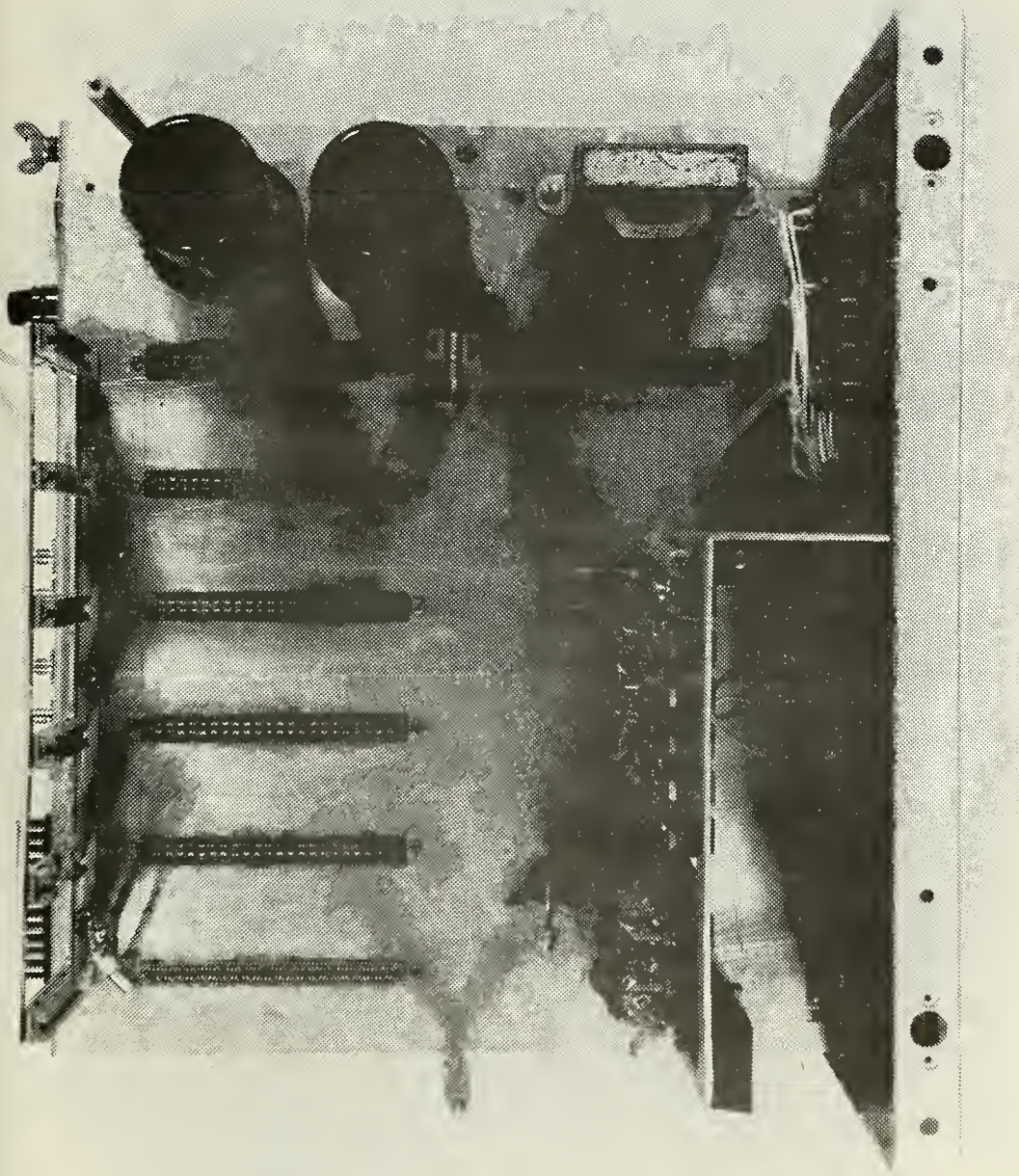
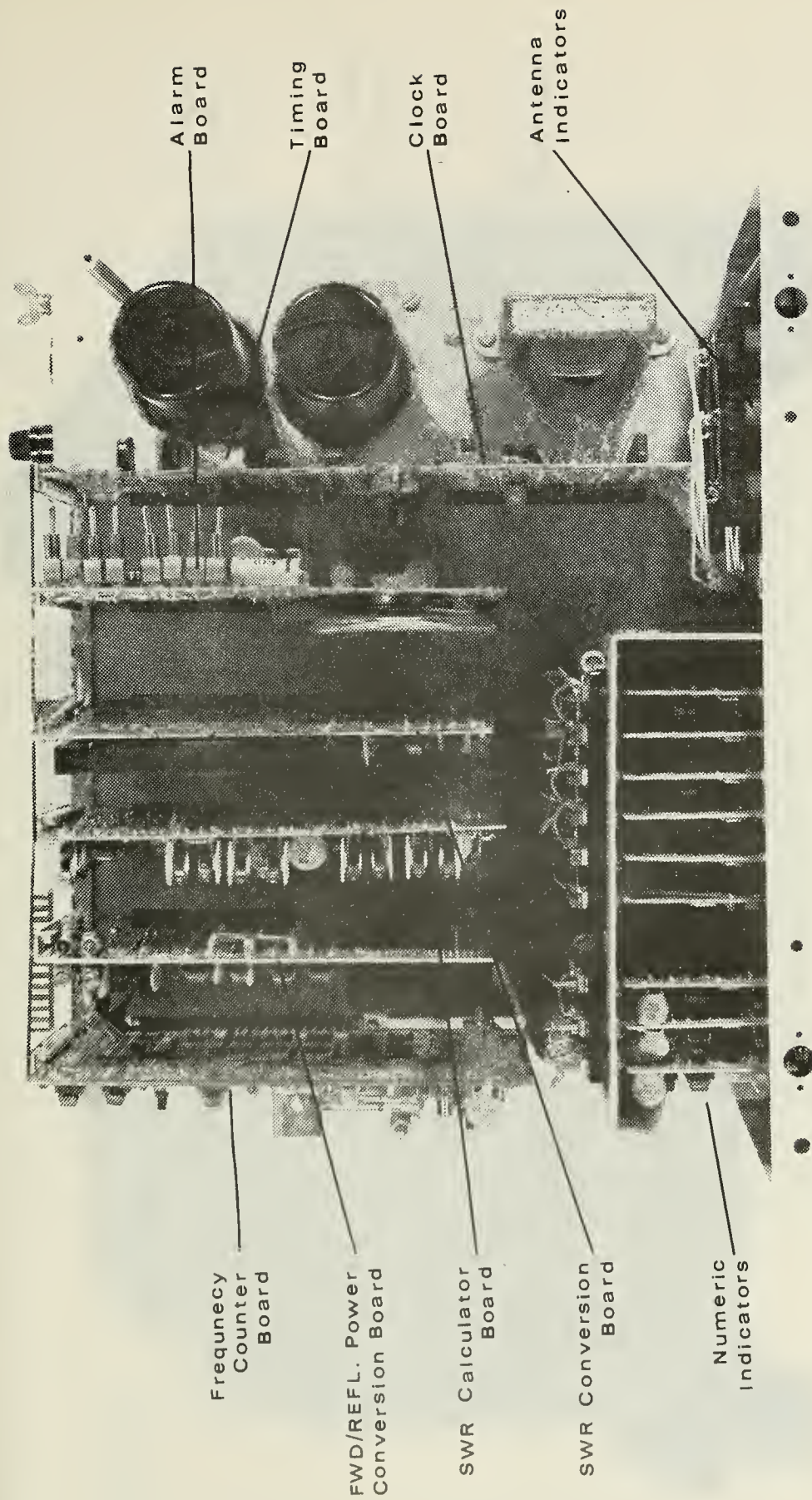


FIGURE 44



MAIN FRAME

FIGURE 46



TOP VIEW

FIGURE 47

Frequency
Counter

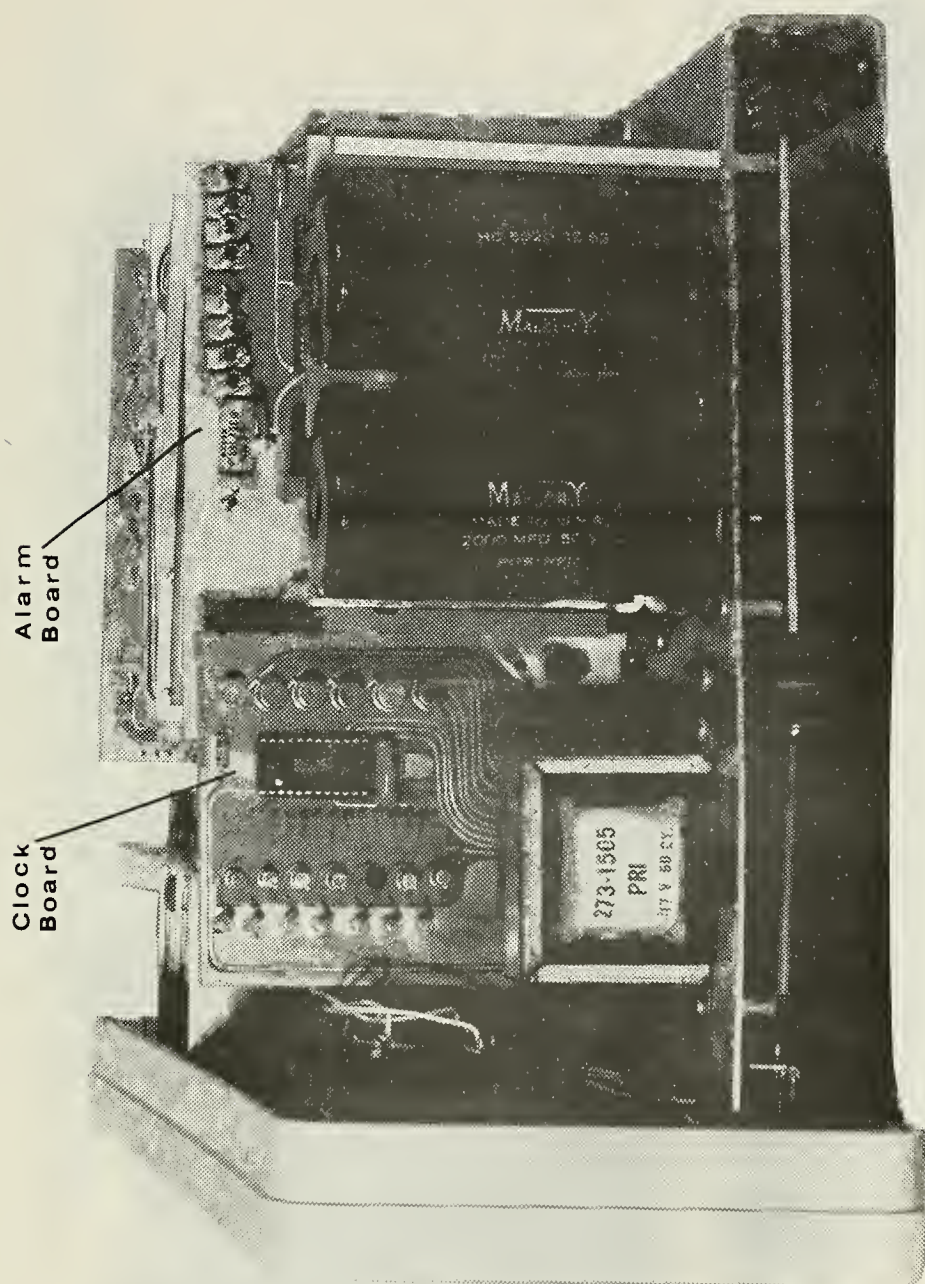
FWD Power
Indicators

REFL. Power
Indicators

SWP
Indicators

RIGHT SIDE VIEW

FIGURE 48



LEFT SIDE VIEW

FIGURE 49

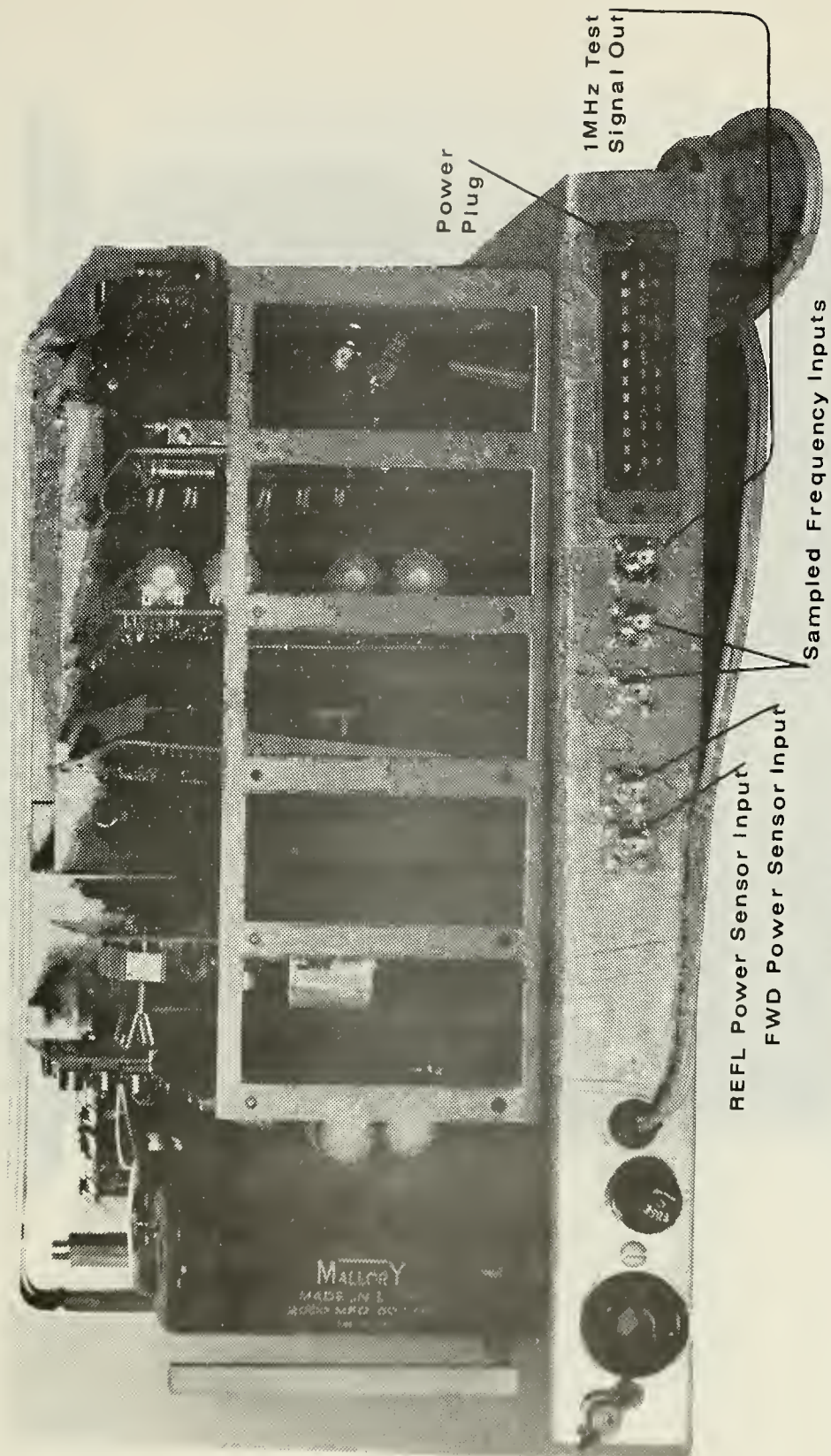
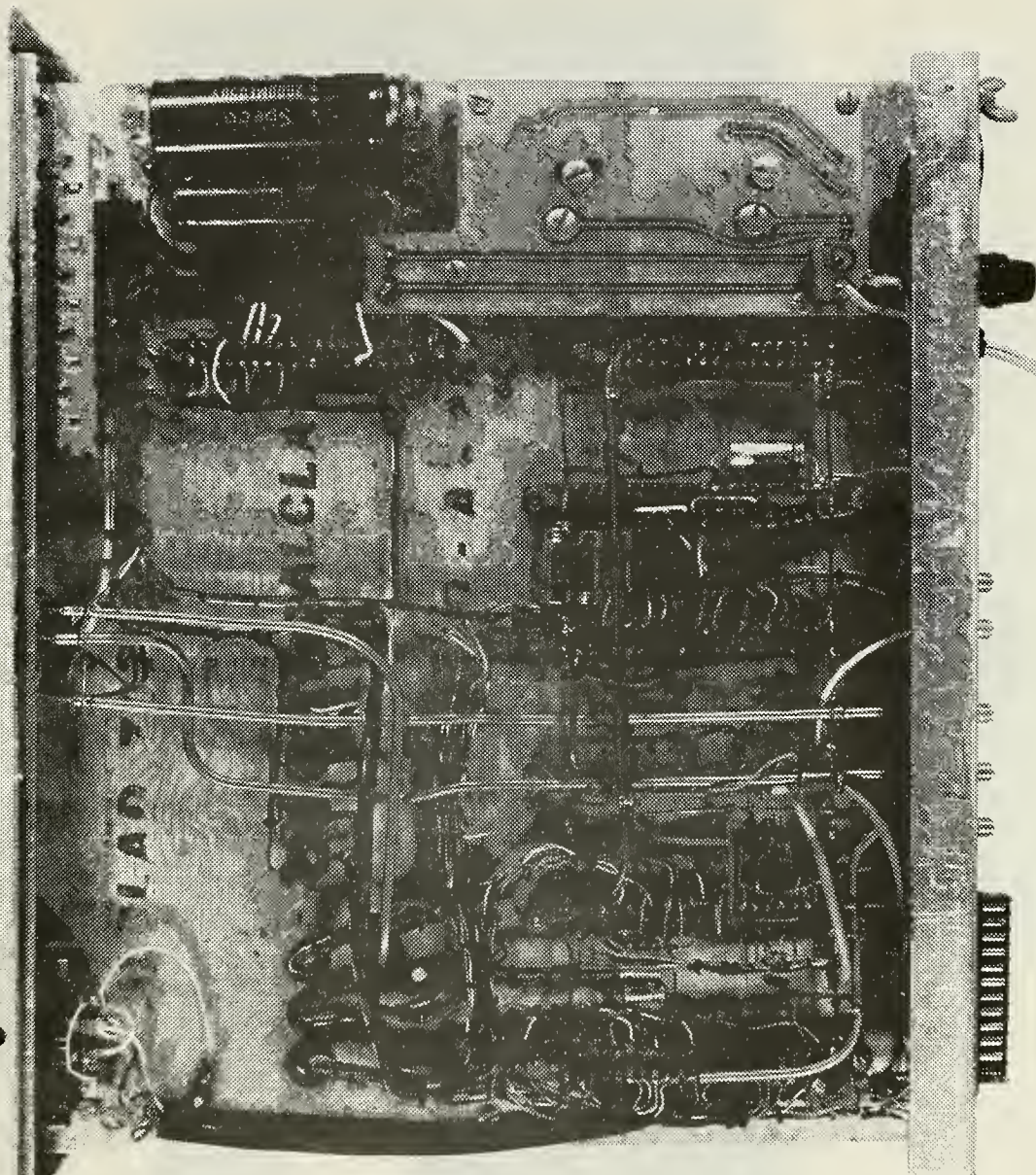


FIGURE 50



BOTTOM VIEW

FIGURE 51

Phase B-C
Voltage

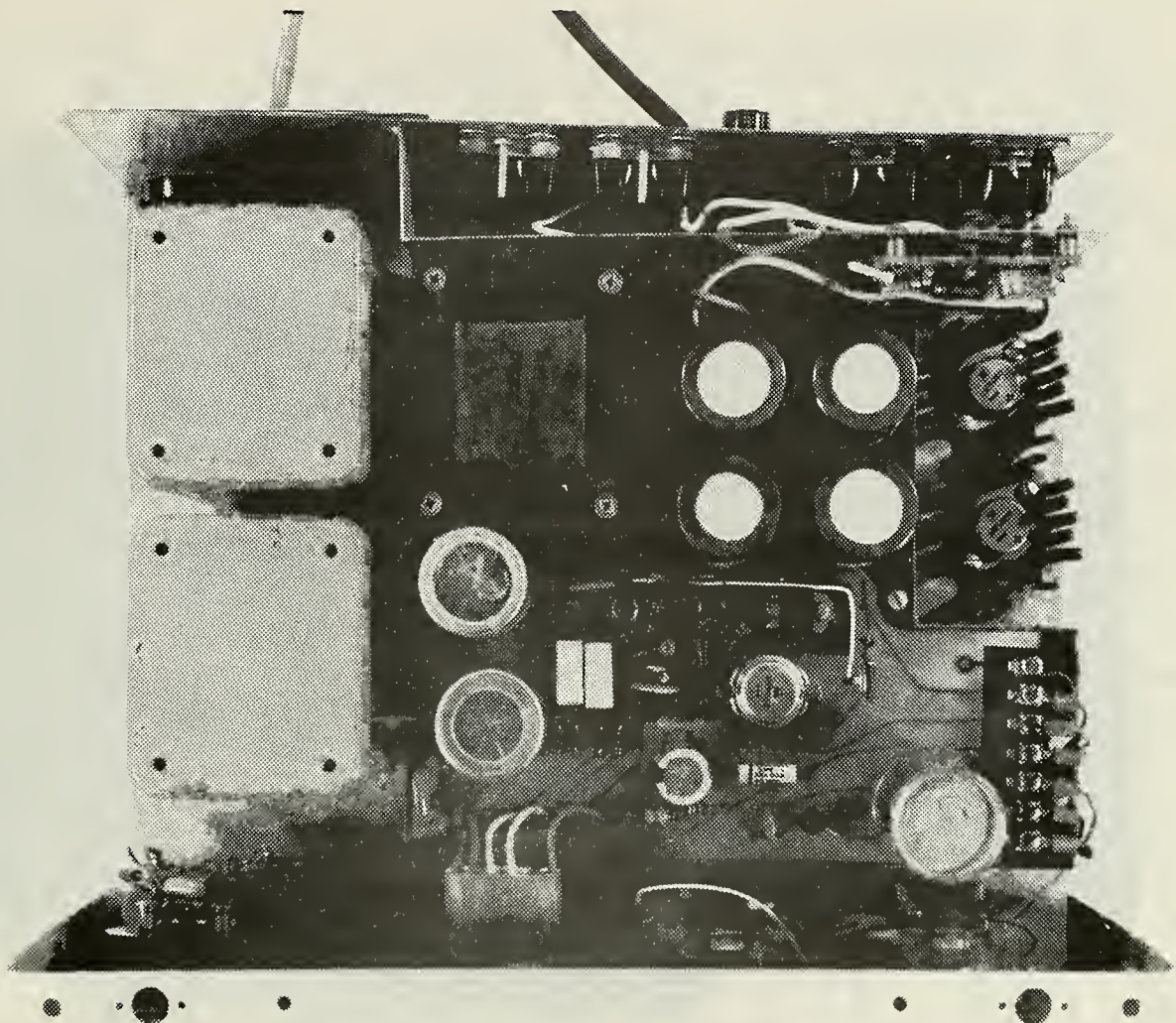
Phase A-B
Voltage

D C Voltage
Monitor

Fuse
D.C. Power
Switch

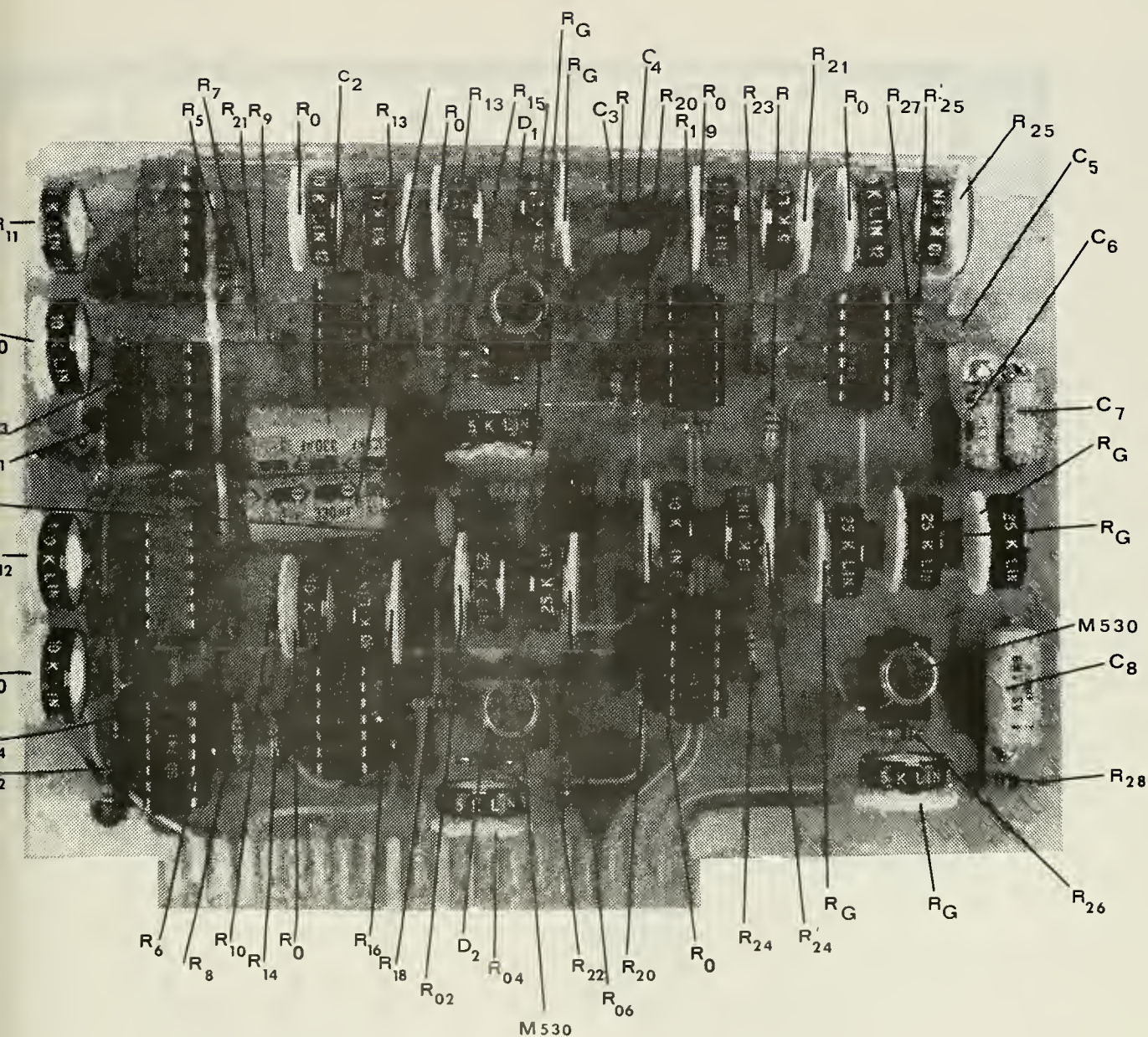
POWER SUPPLY FACE PANEL

FIGURE 52



POWER SUPPLY TOP VIEW

FIGURE 53



R_G ... Gain Bias Adjustment

R_0 ... Zero Offset Adjust

SWR CALCULATOR

FIGURE 54

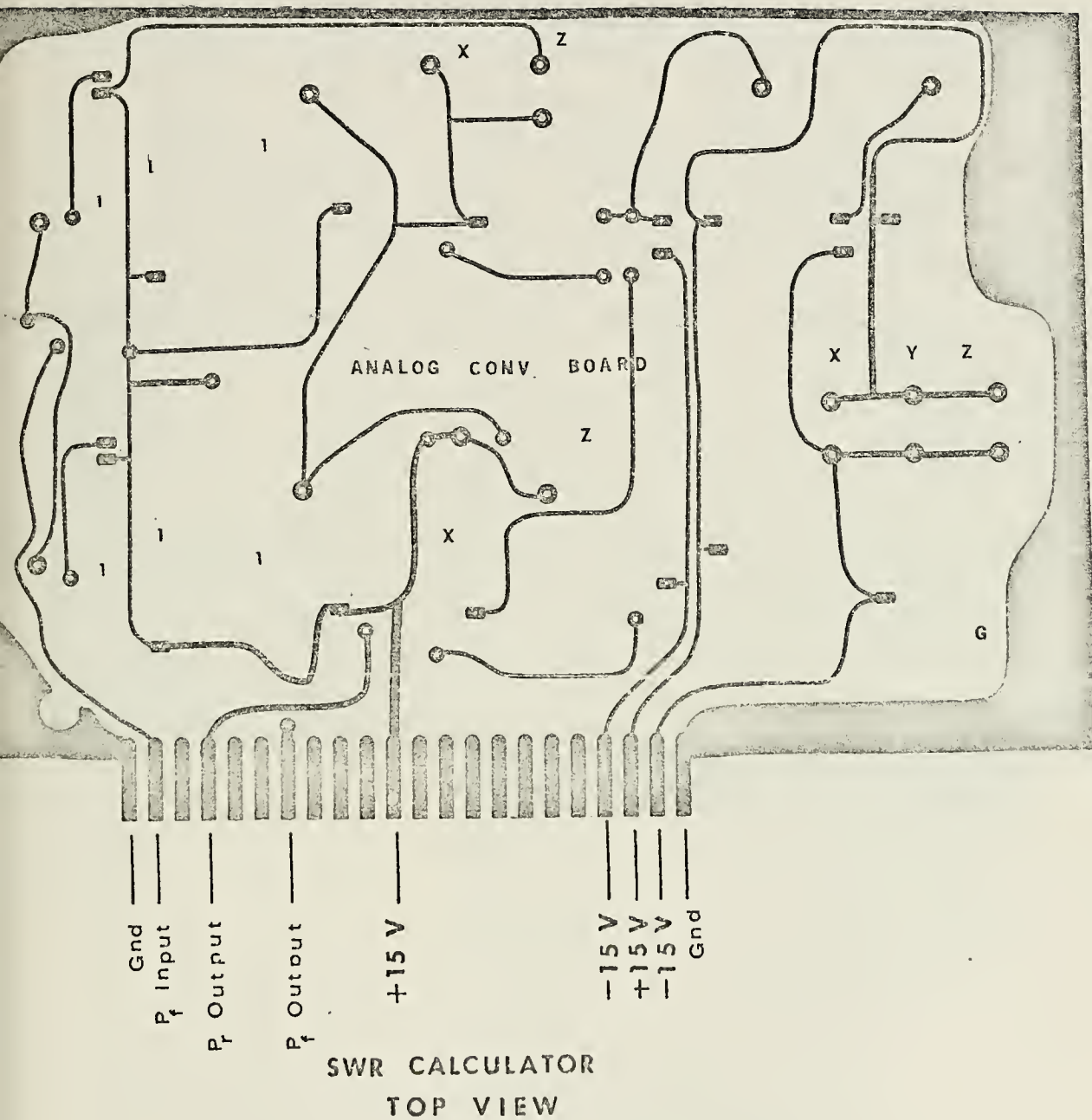


FIGURE 55

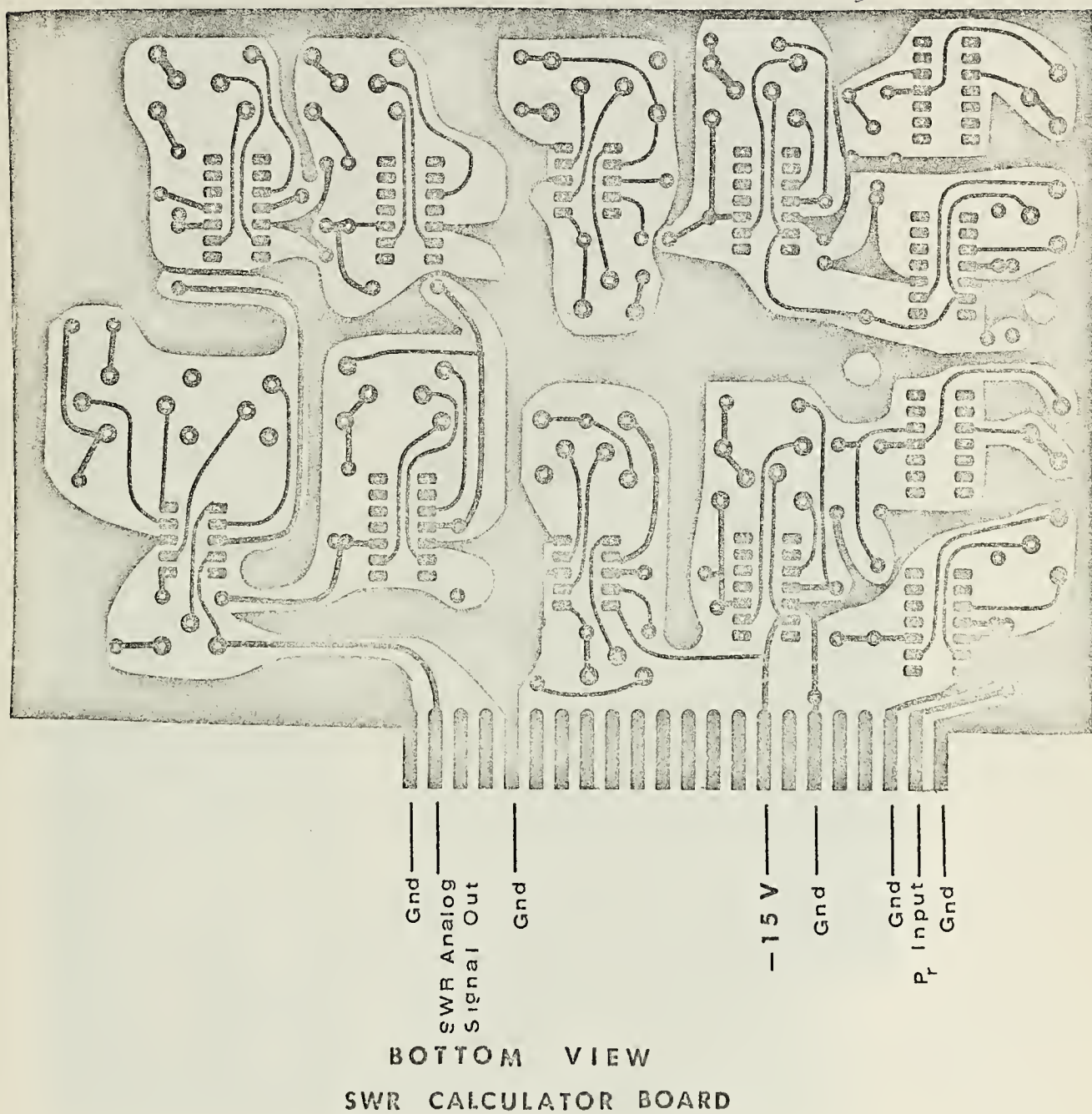
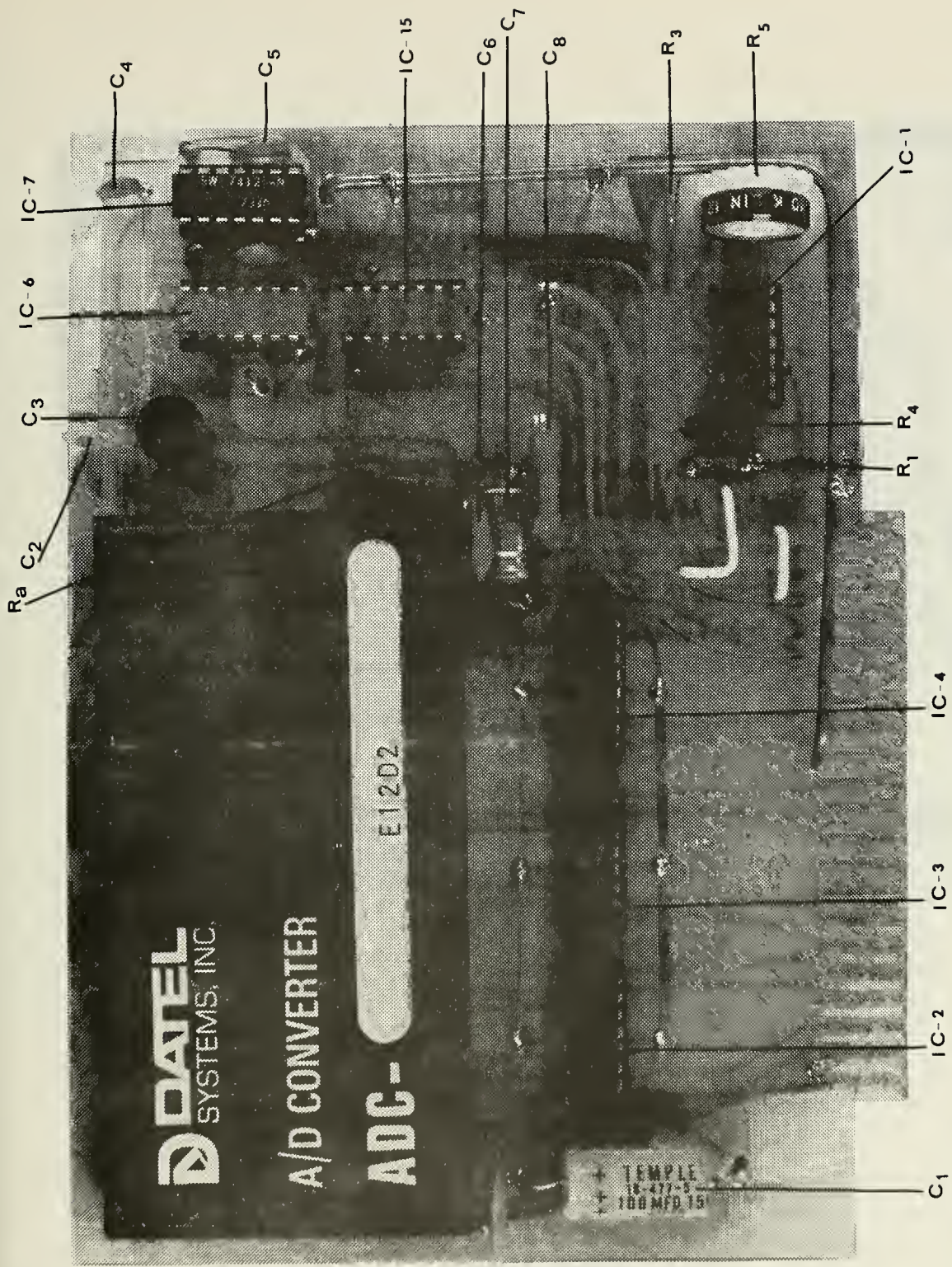
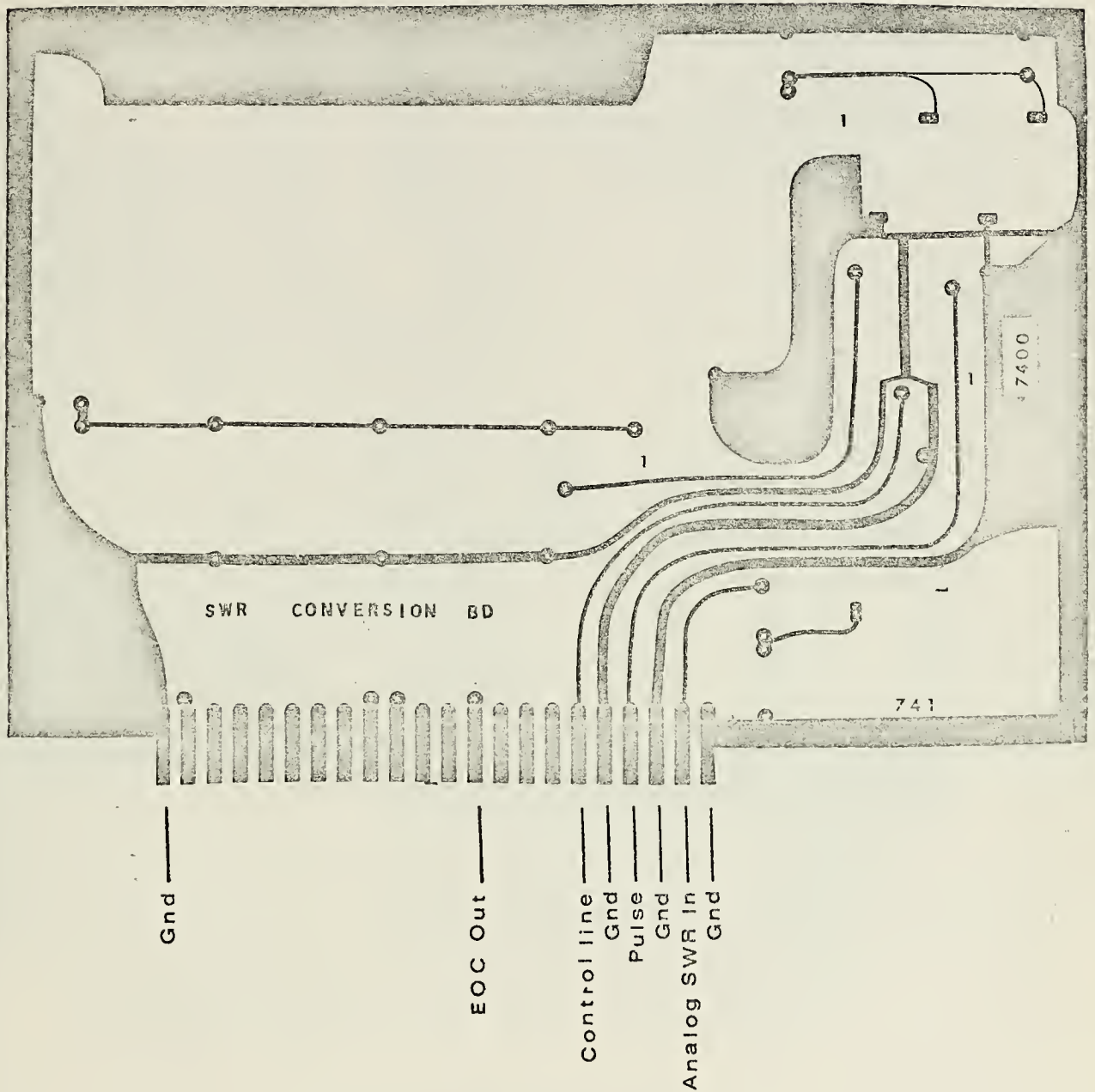


FIGURE 56



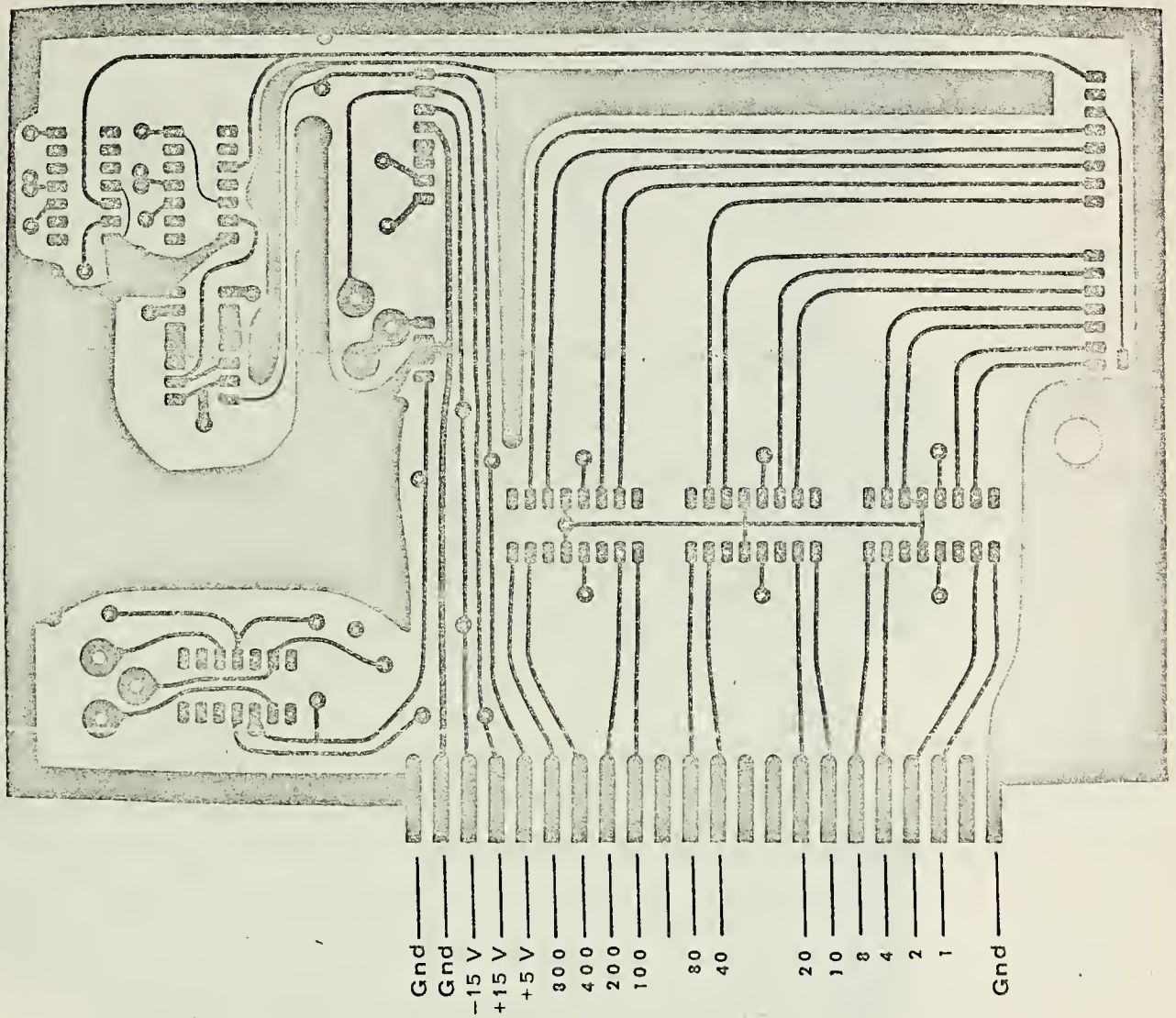
SWR CONVERSION BOARD

FIGURE 57



SWR CONVERSION BOARD
TOP VIEW

FIGURE 58



SWR CONVERSION BOARD
BOTTOM VIEW

FIGURE 59

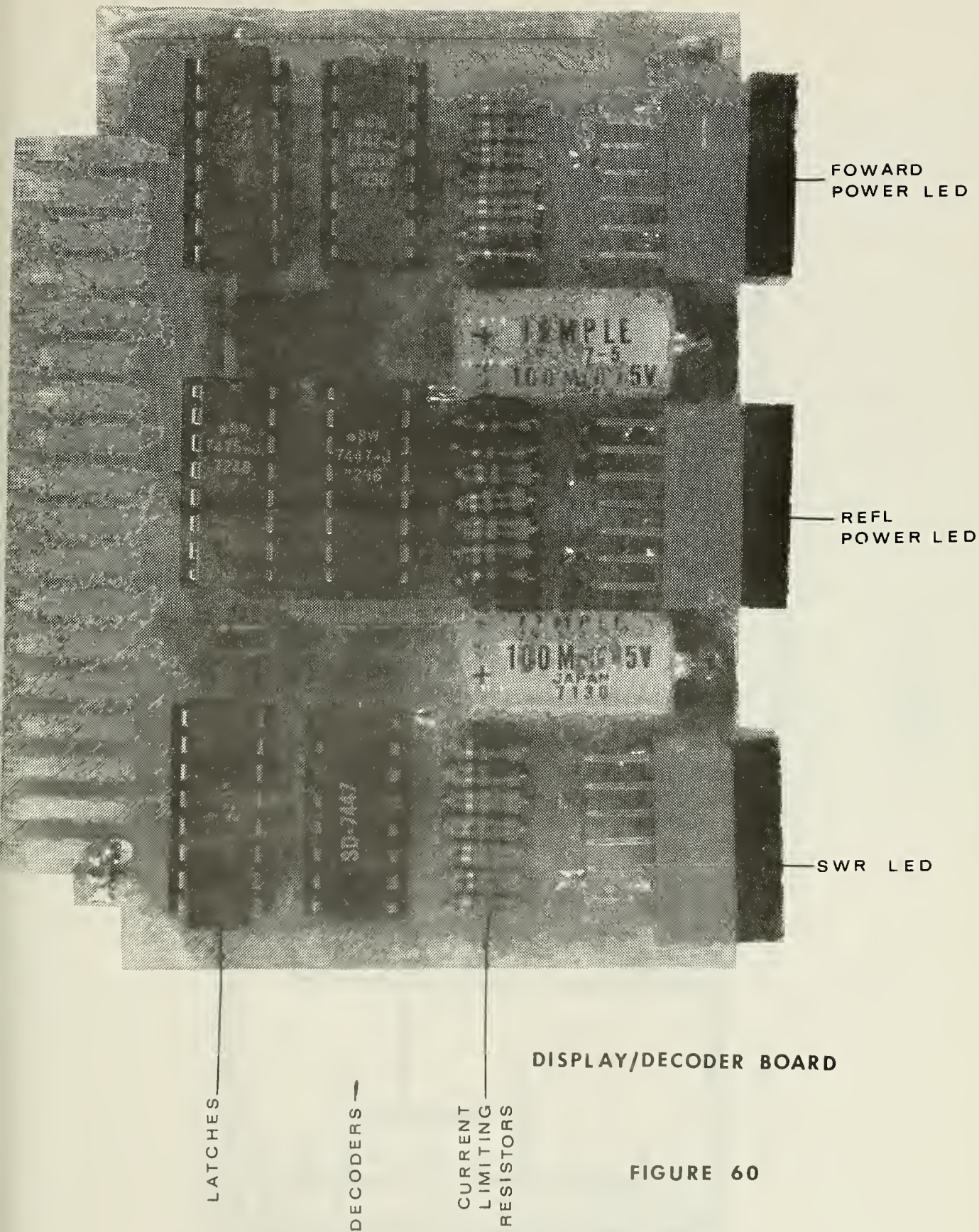
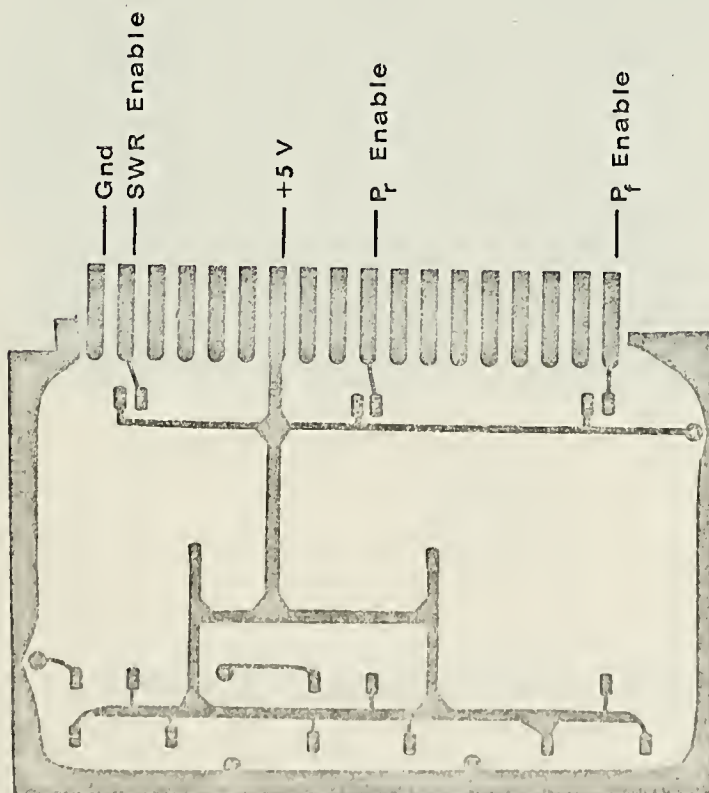
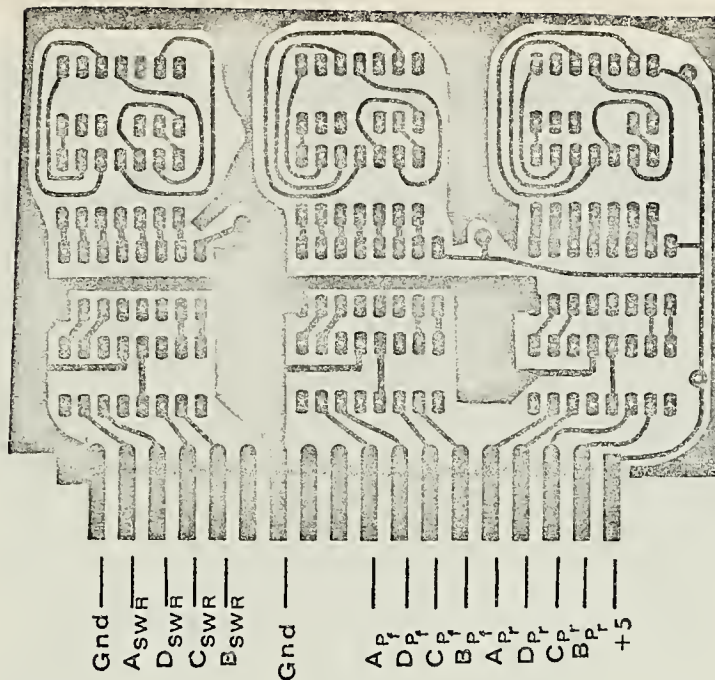


FIGURE 60



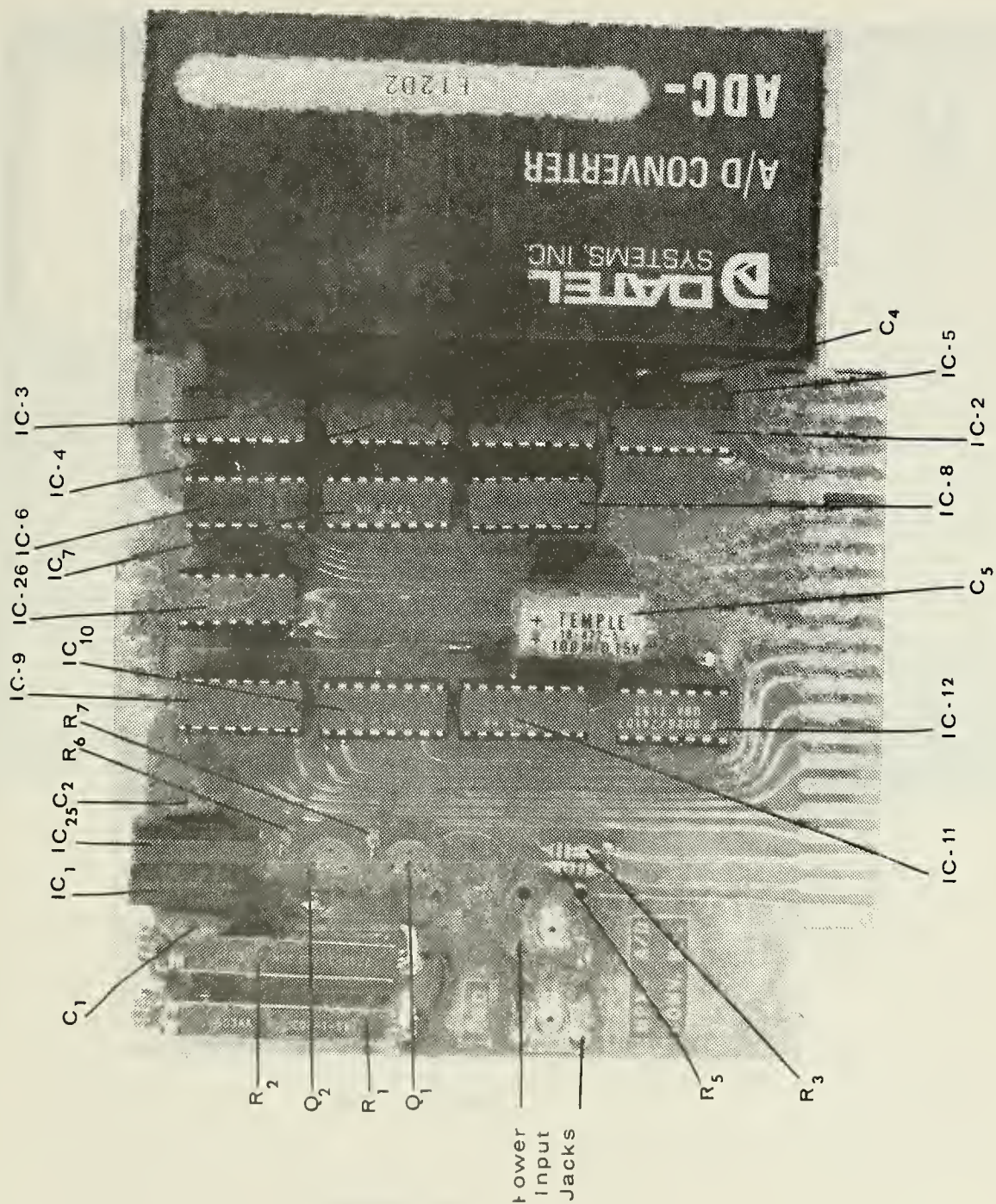
TOP VIEW



BOTTOM VIEW

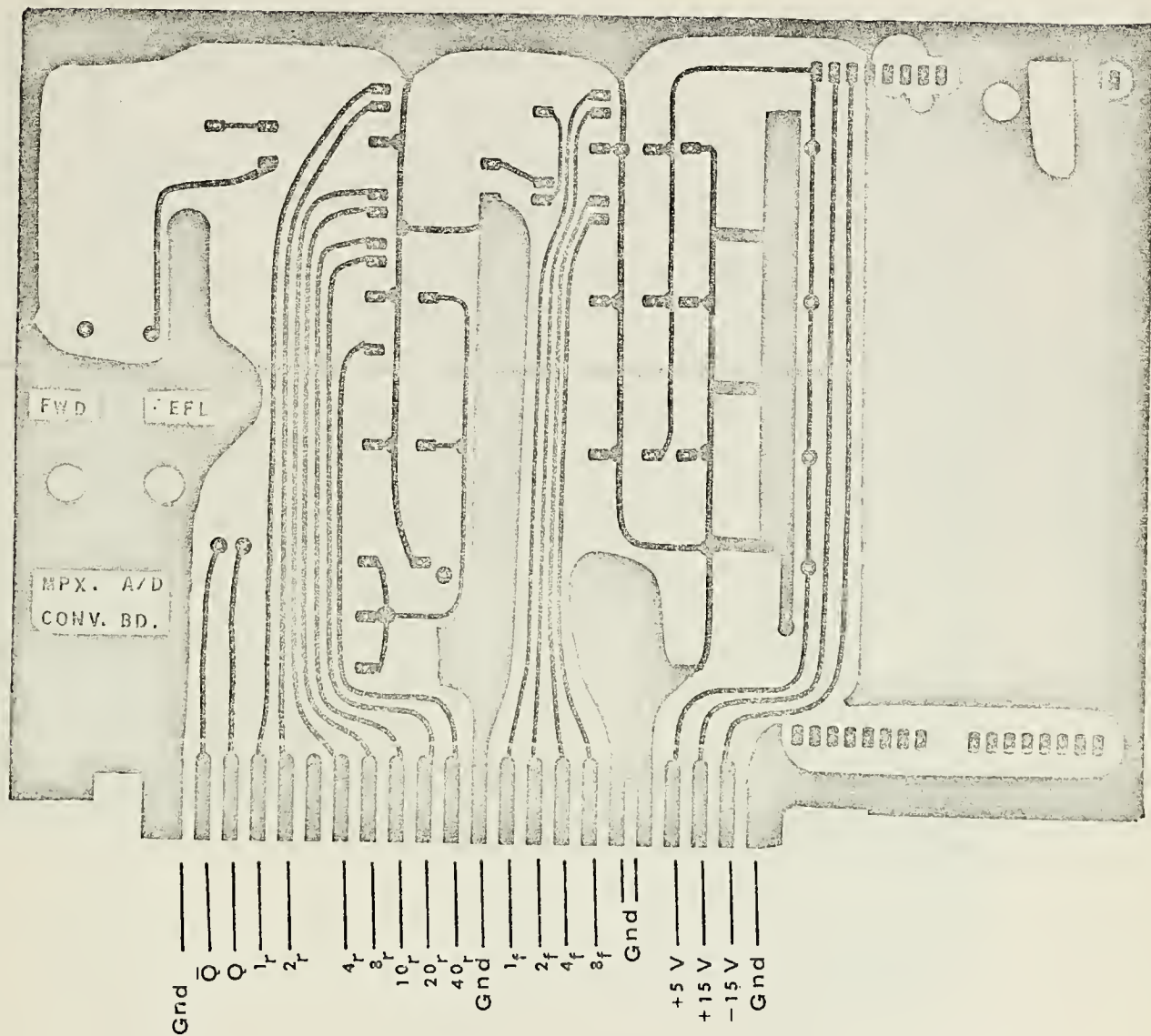
DISPLAY/DECODER BOARD

FIGURE 61



FORWARD/REFLECTED POWER BOARD

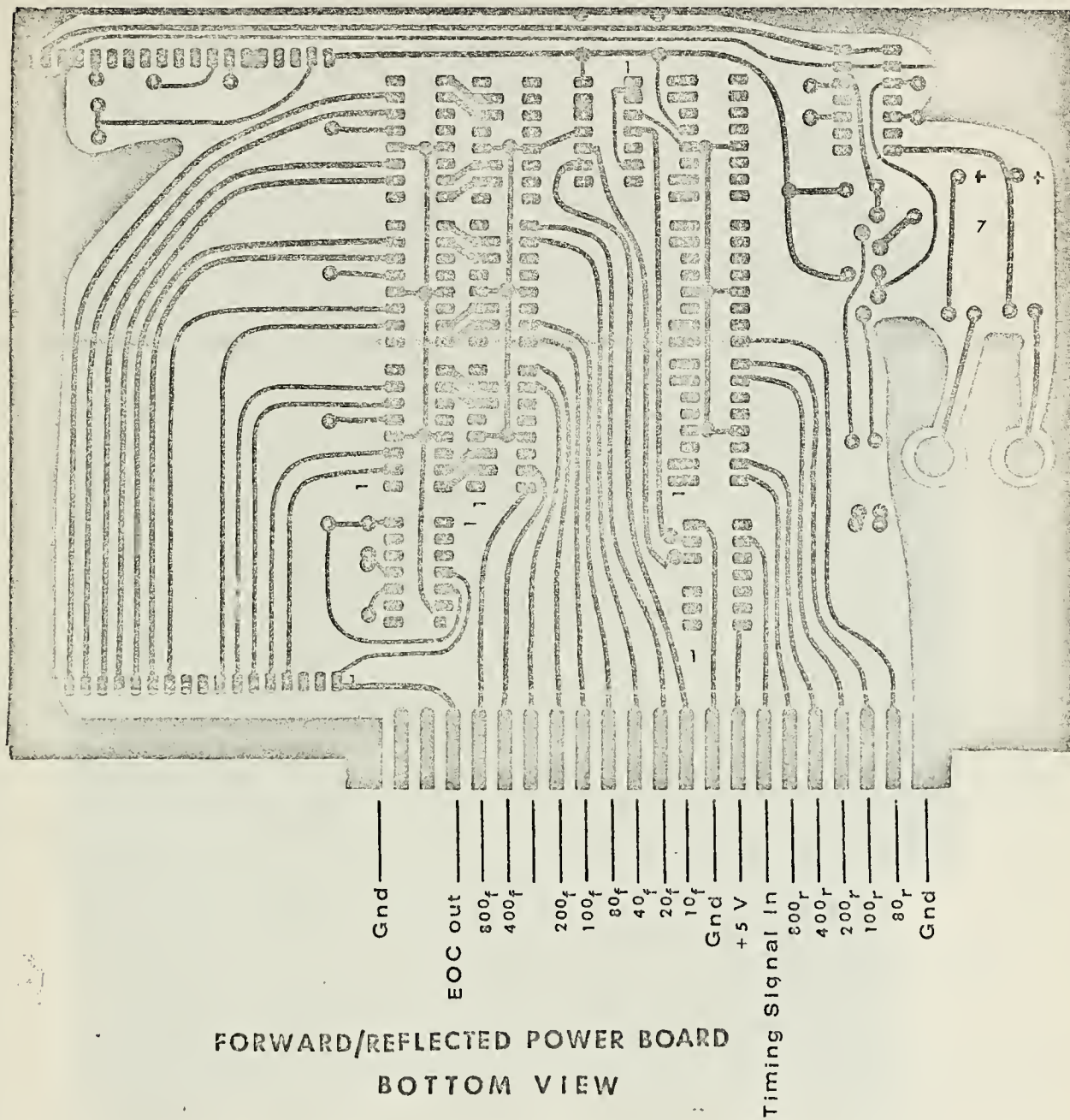
FIGURE 62



FORWARD/REFLECTED POWER BOARD

TOP VIEW

FIGURE 63



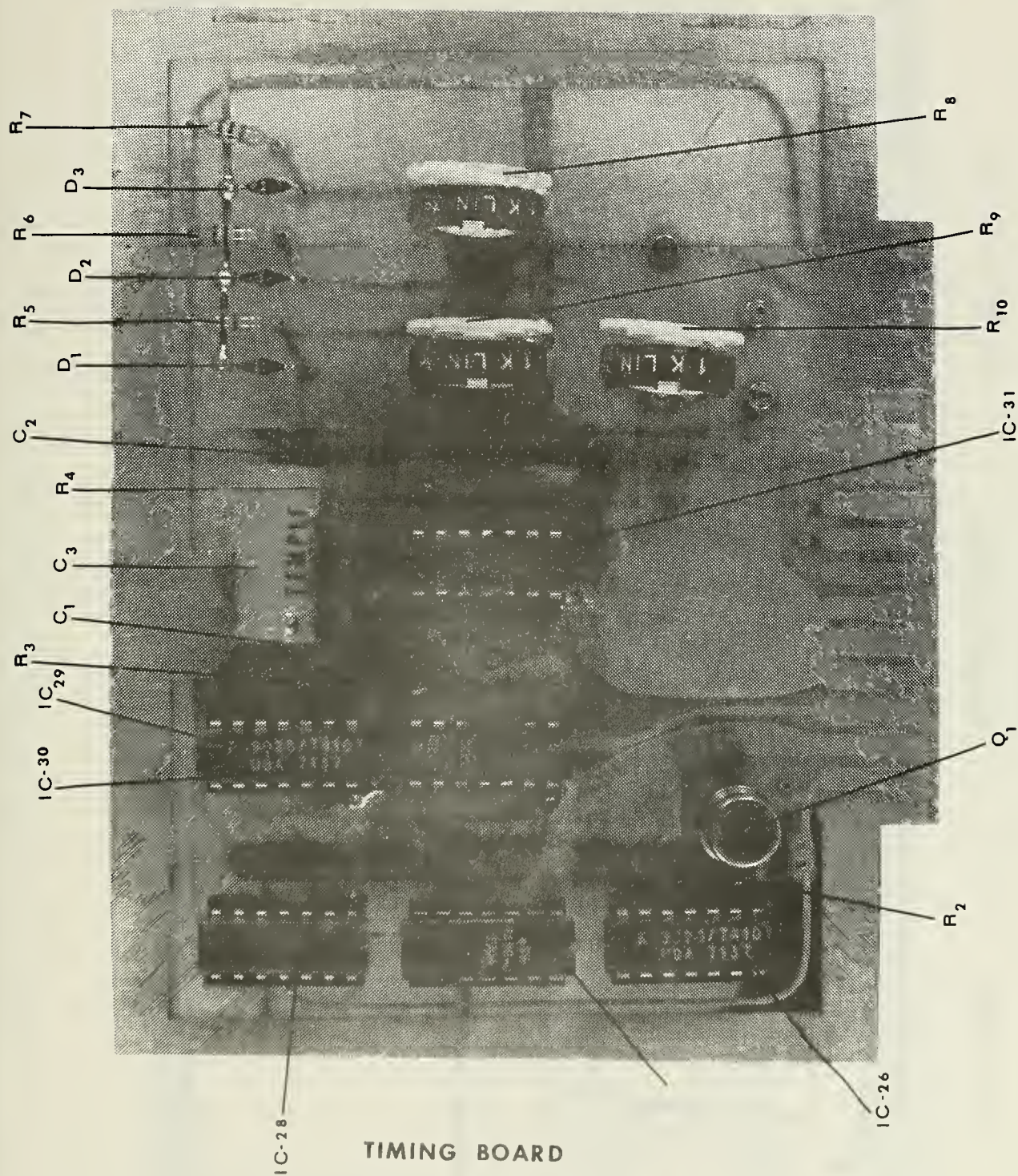
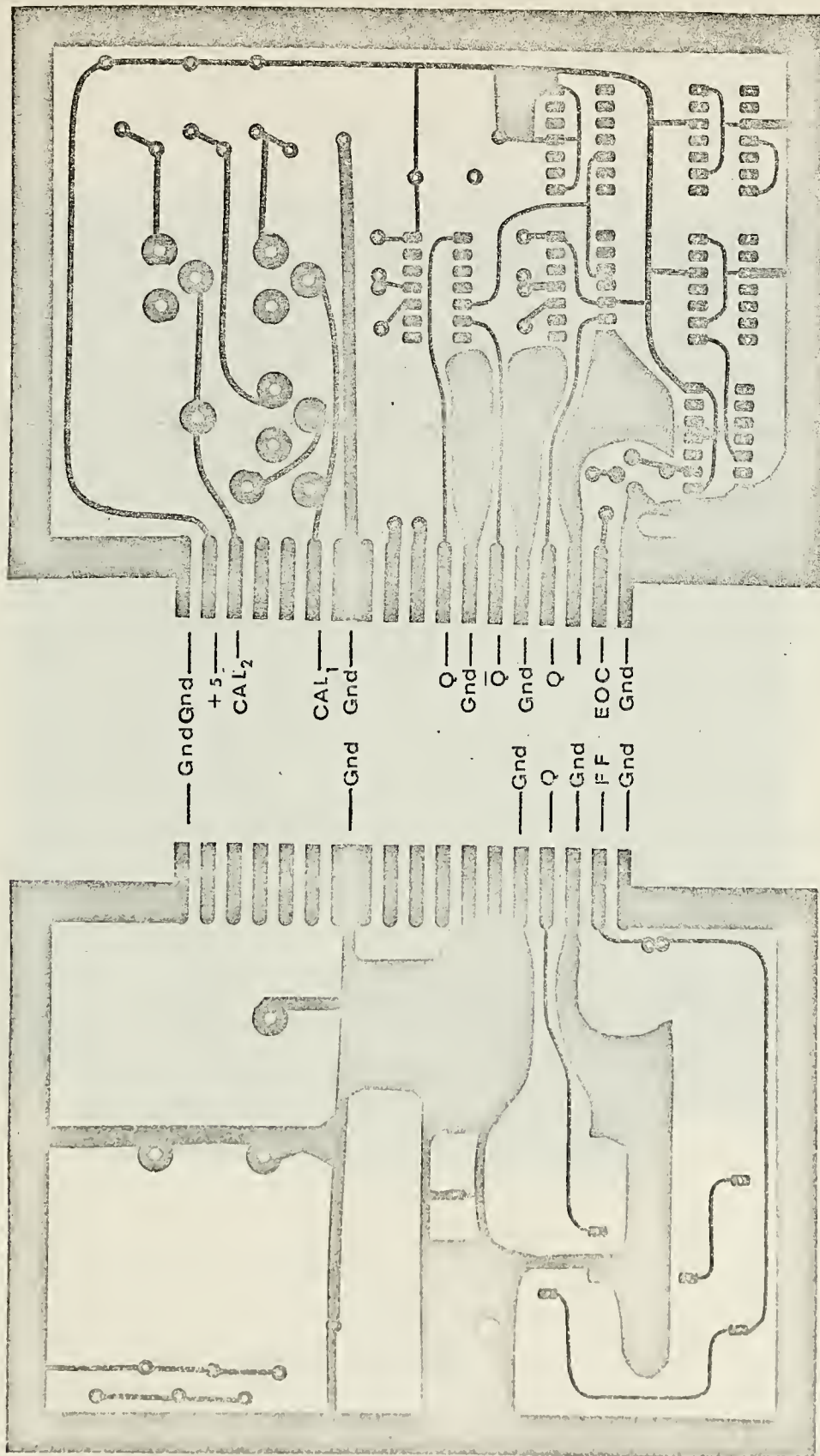


FIGURE 65

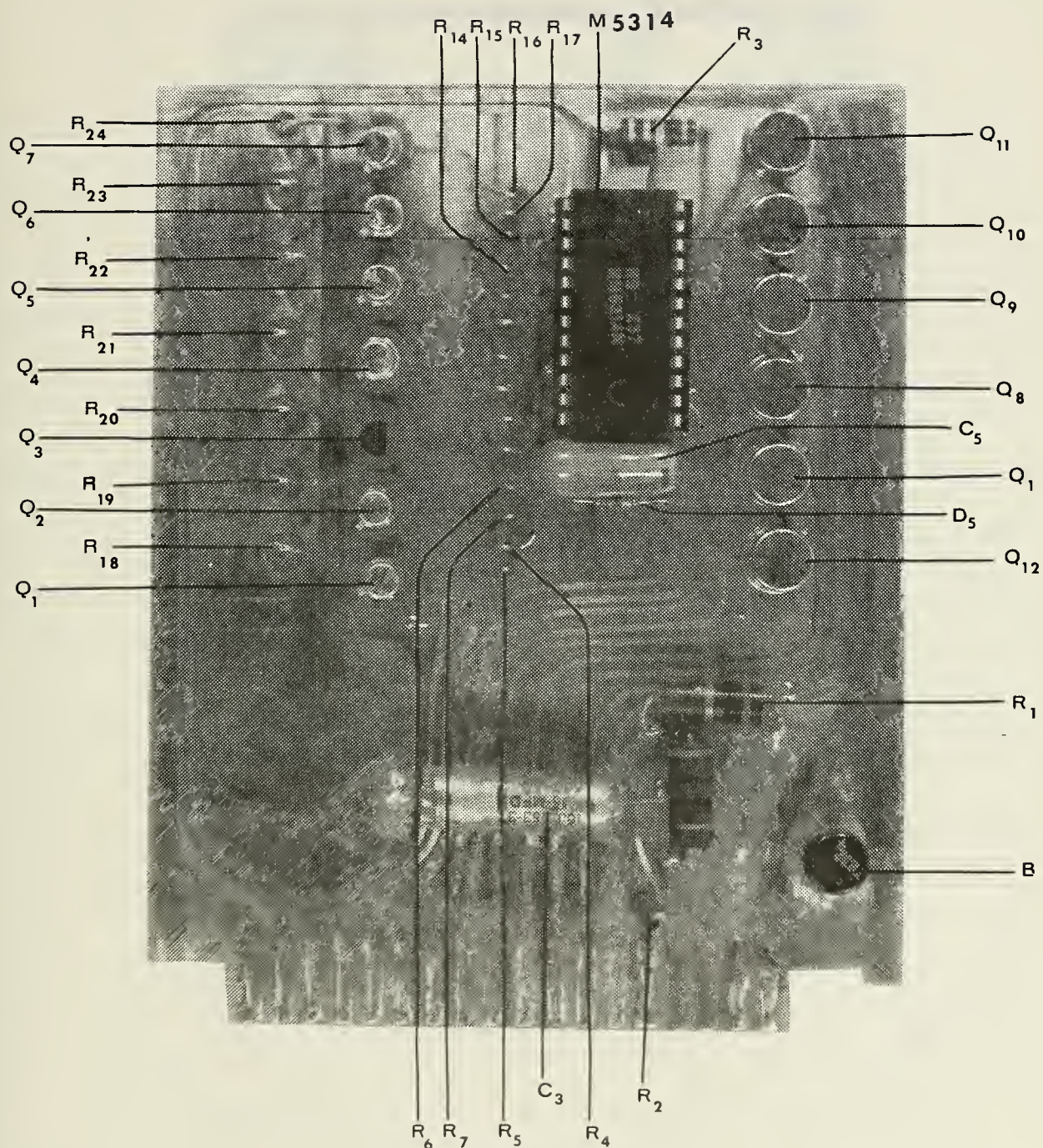


TOP VIEW

TIMING BOARD

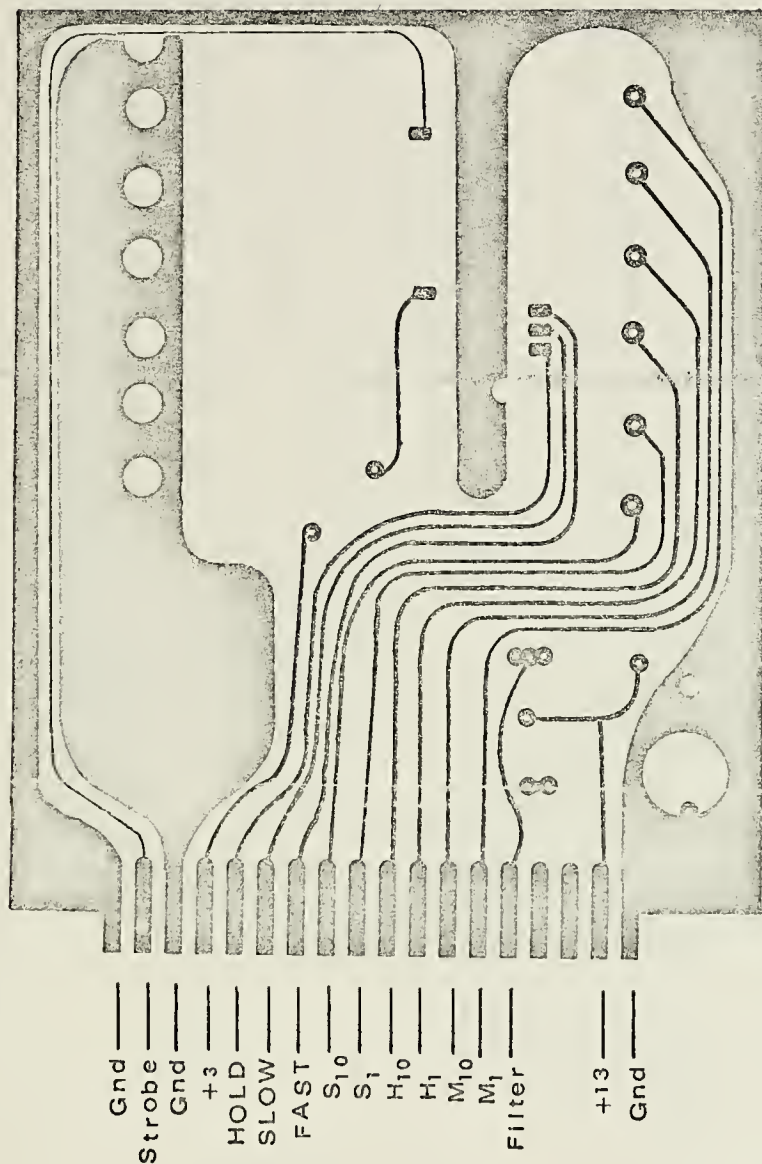
BOTTOM VIEW

FIGURE 66



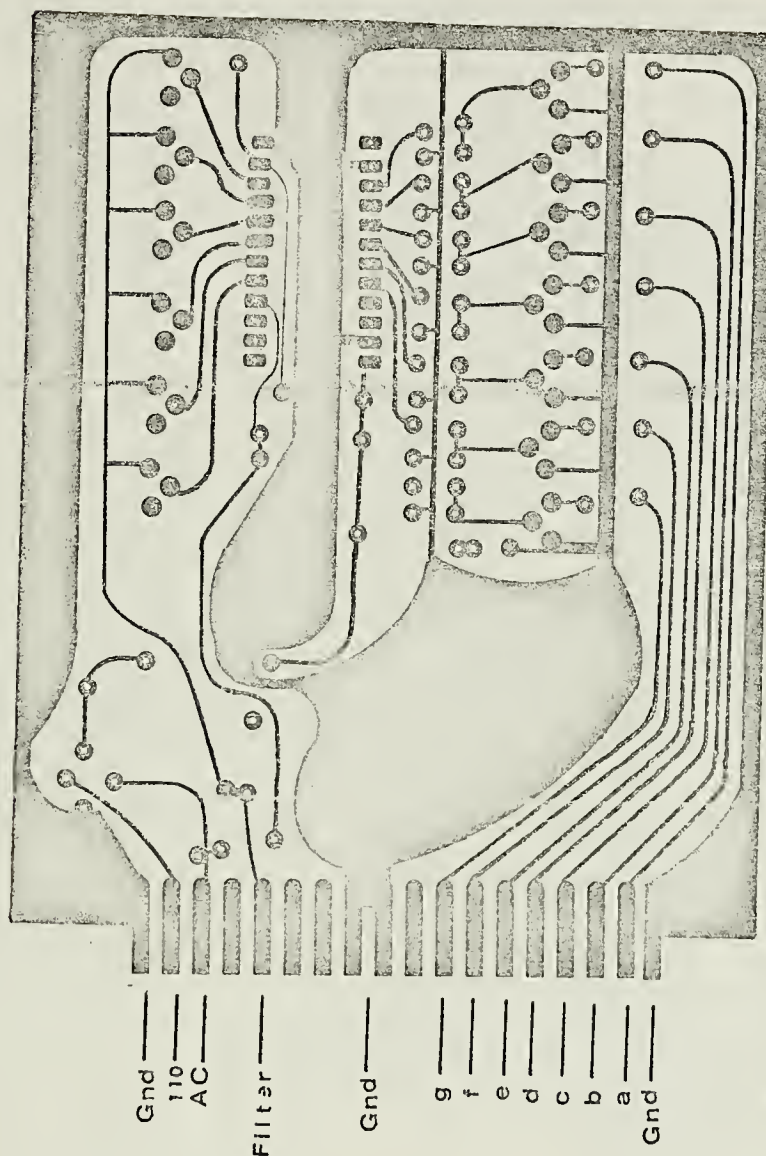
DIGITAL CLOCK

FIGURE 67



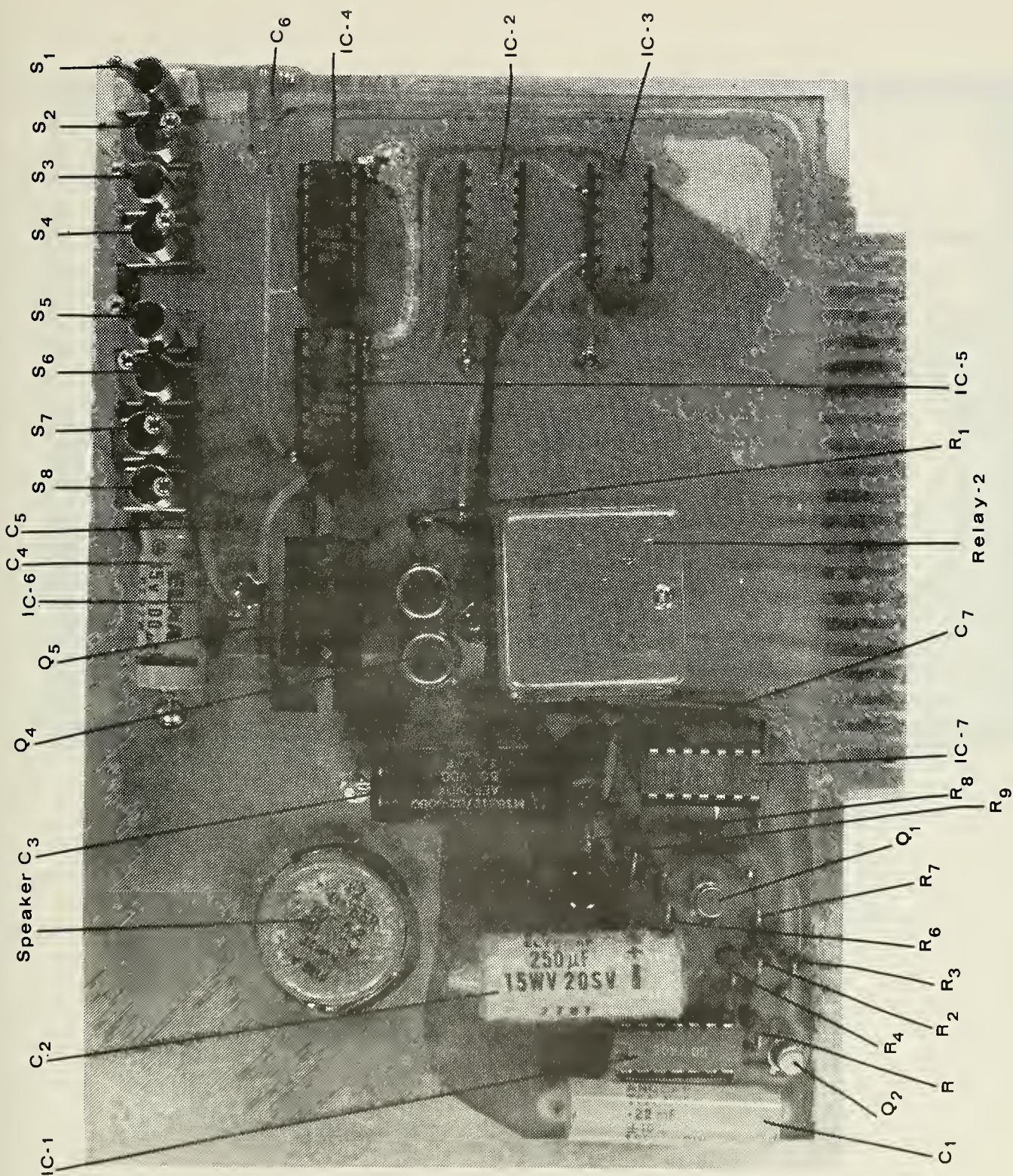
DIGITAL CLOCK
TOP VIEW

FIGURE 68



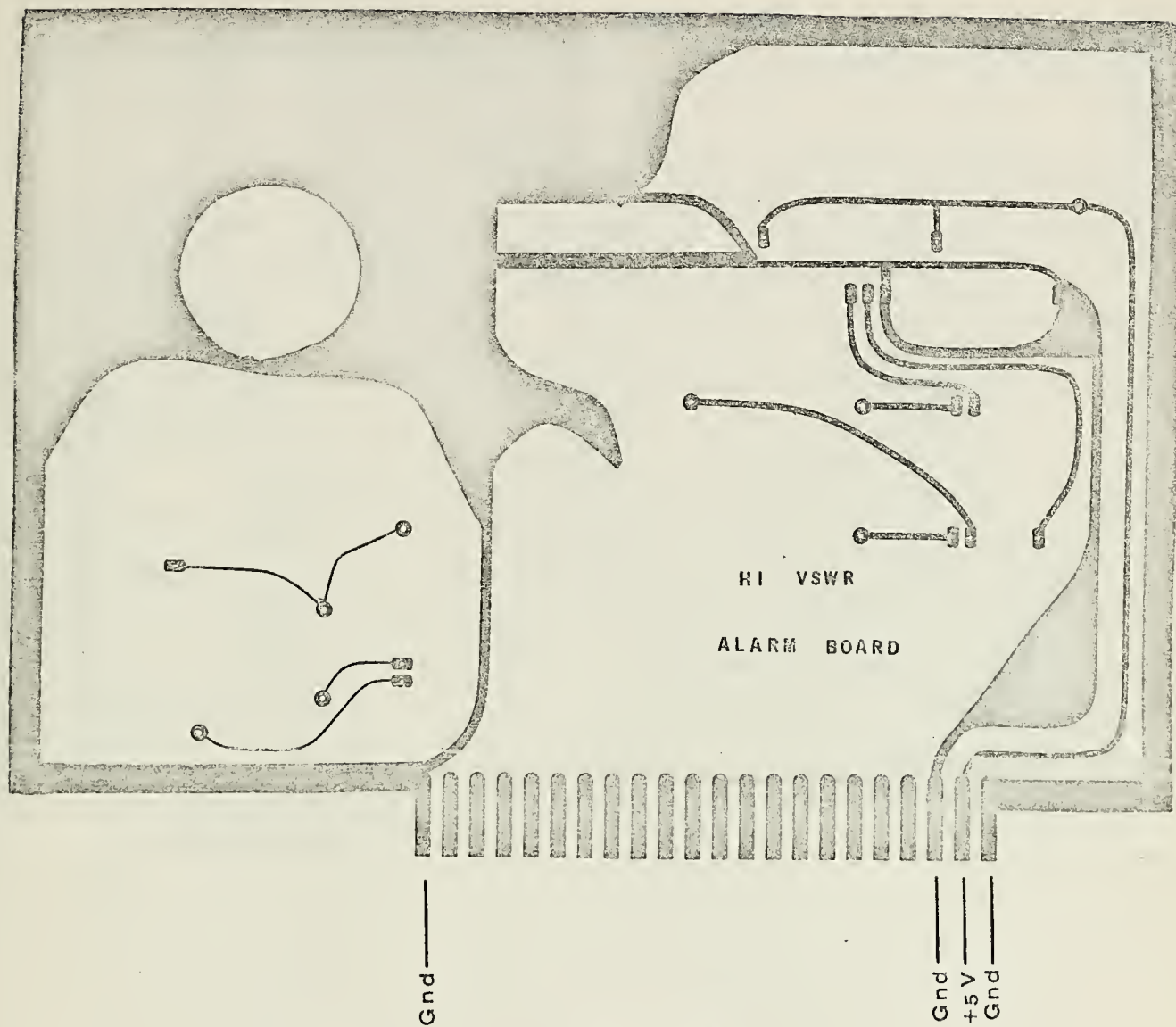
DIGITAL CLOCK
BOTTOM VIEW

FIGURE 69



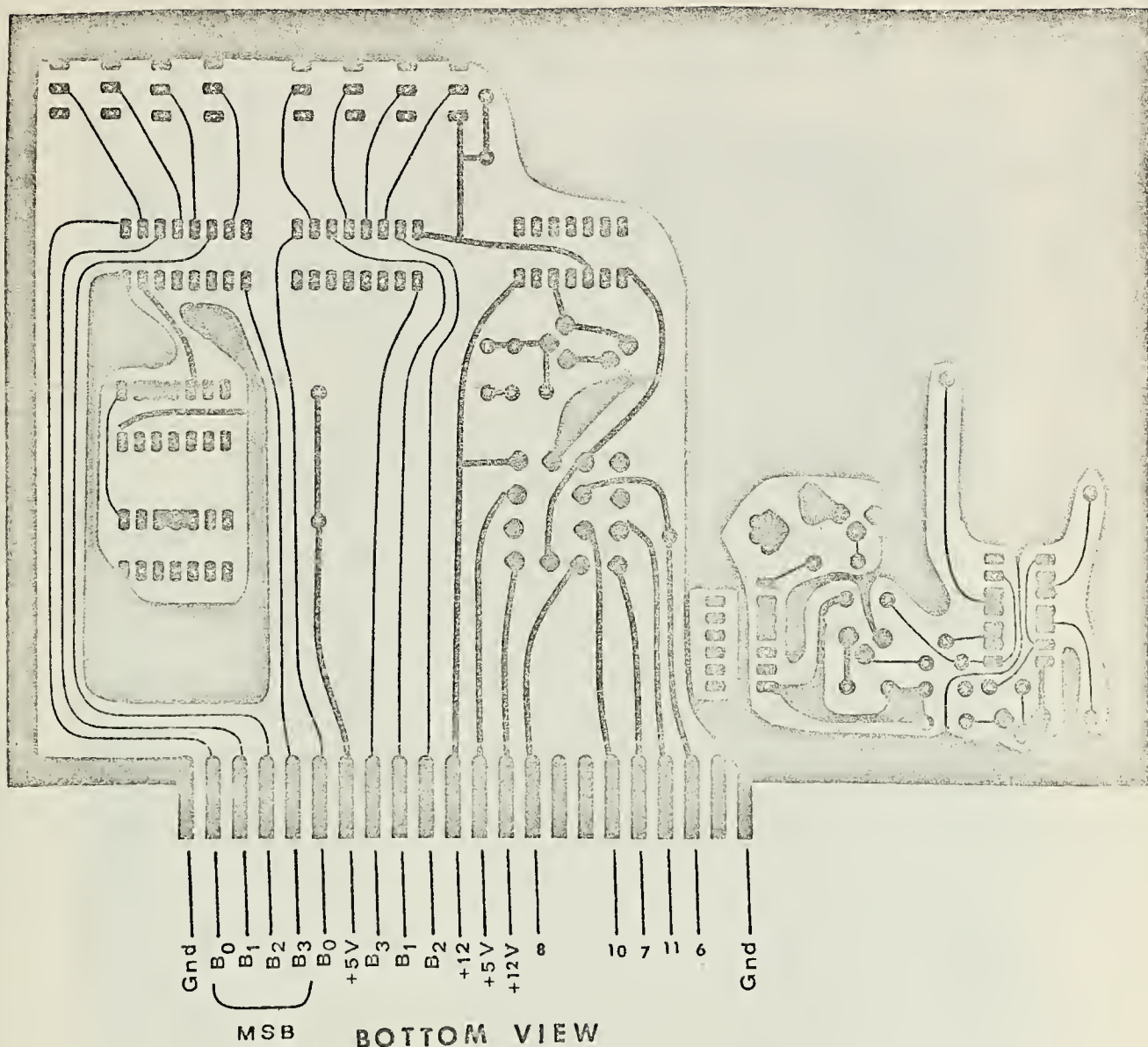
SWR ALARM BOARD

FIGURE 70



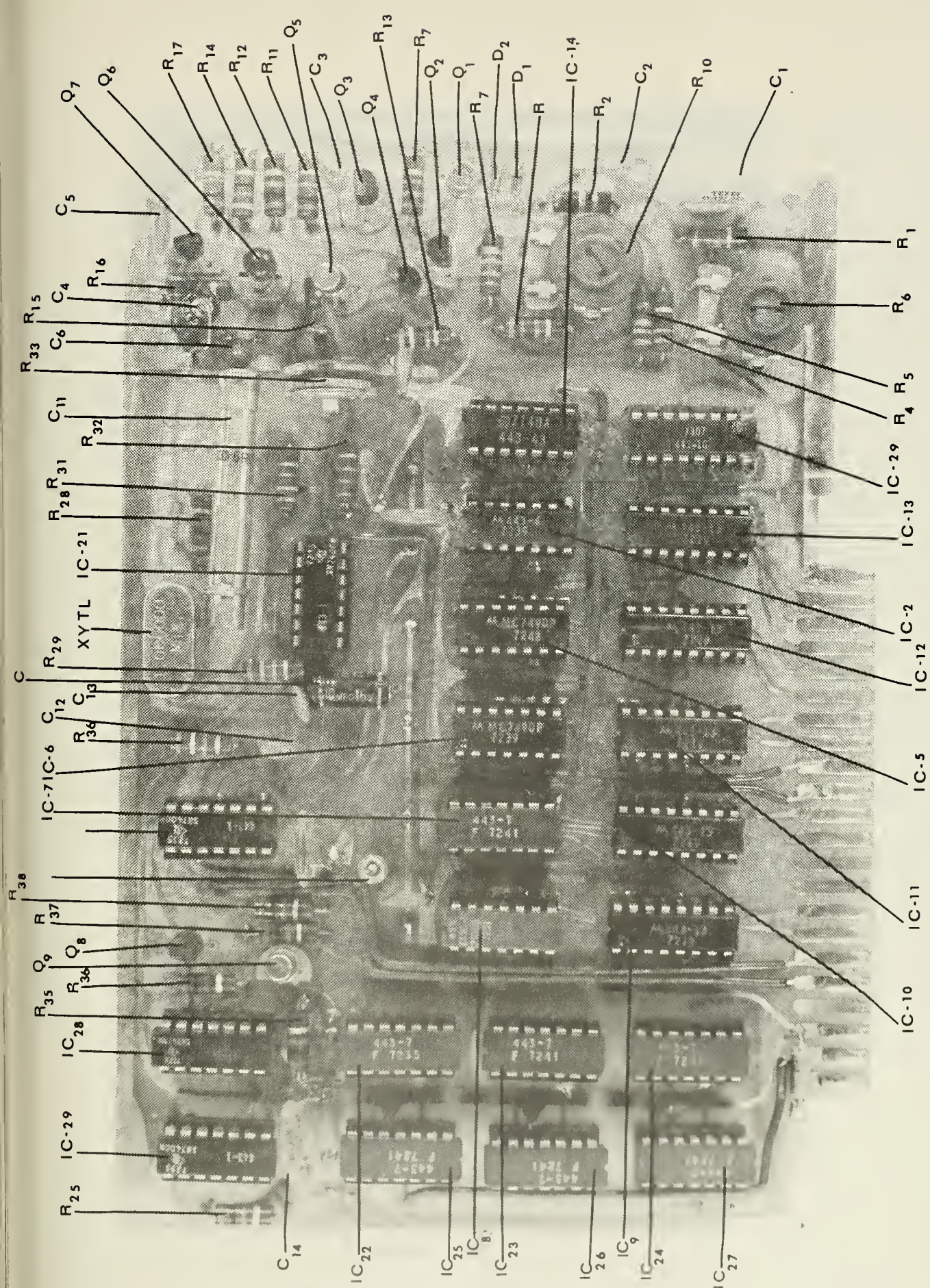
TOP VIEW
SWR ALARM BOARD

FIGURE 71

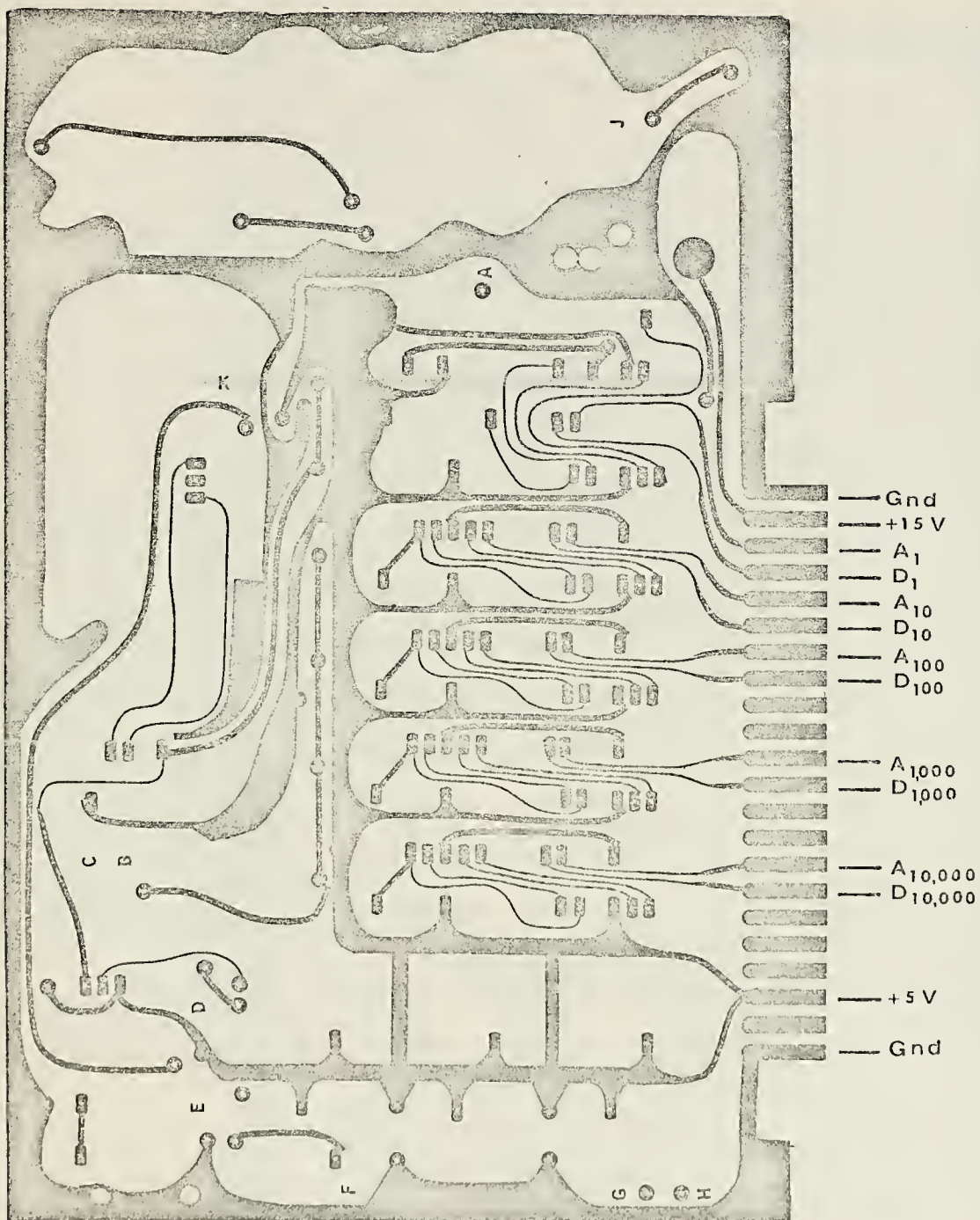


SWR ALARM BOARD

FIGURE 72

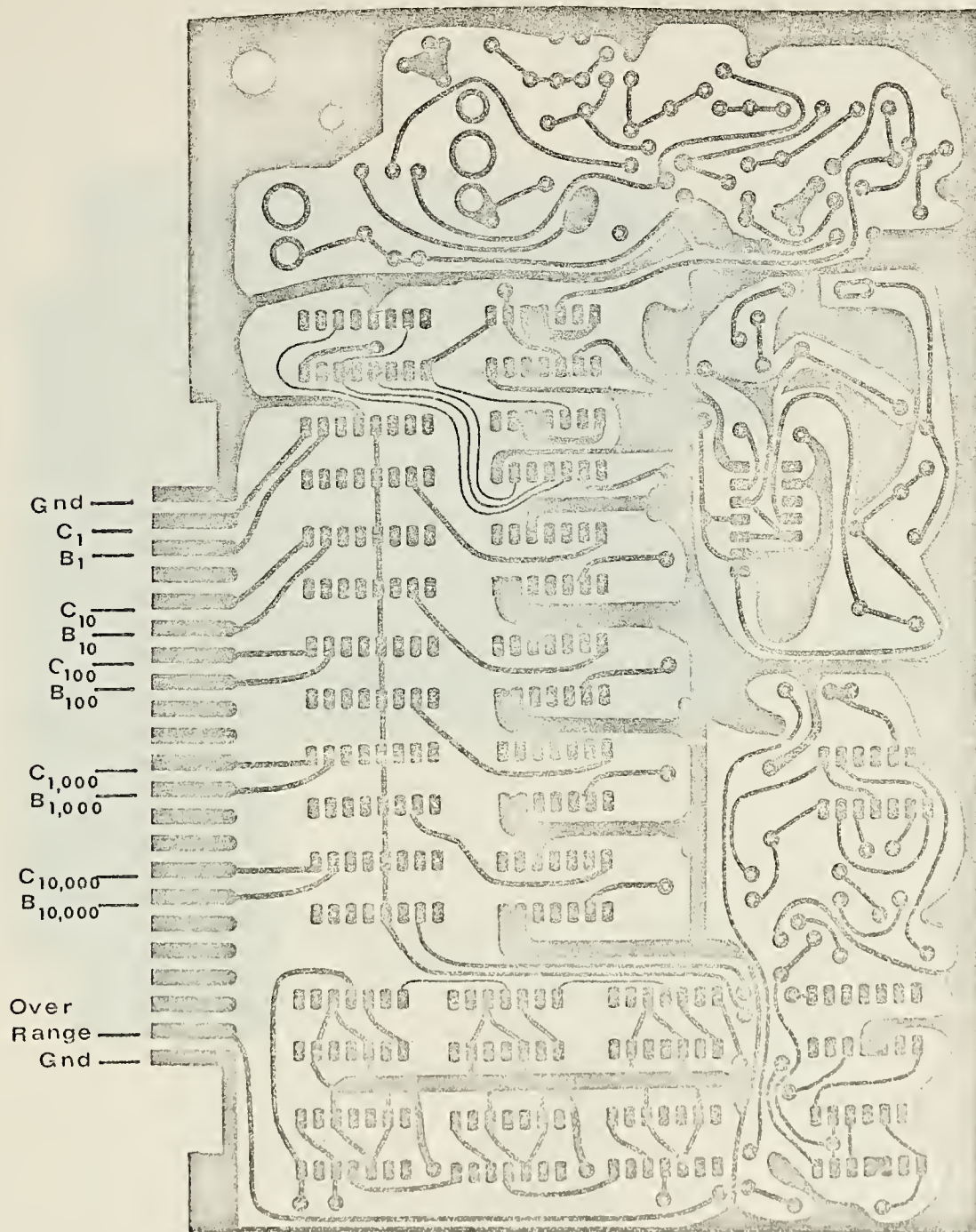


FREQUENCY COUNTER



TOP VIEW
FREQUENCY COUNTER

FIGURE 74



BOTTOM VIEW
FREQUENCY COUNTER

FIGURE 75

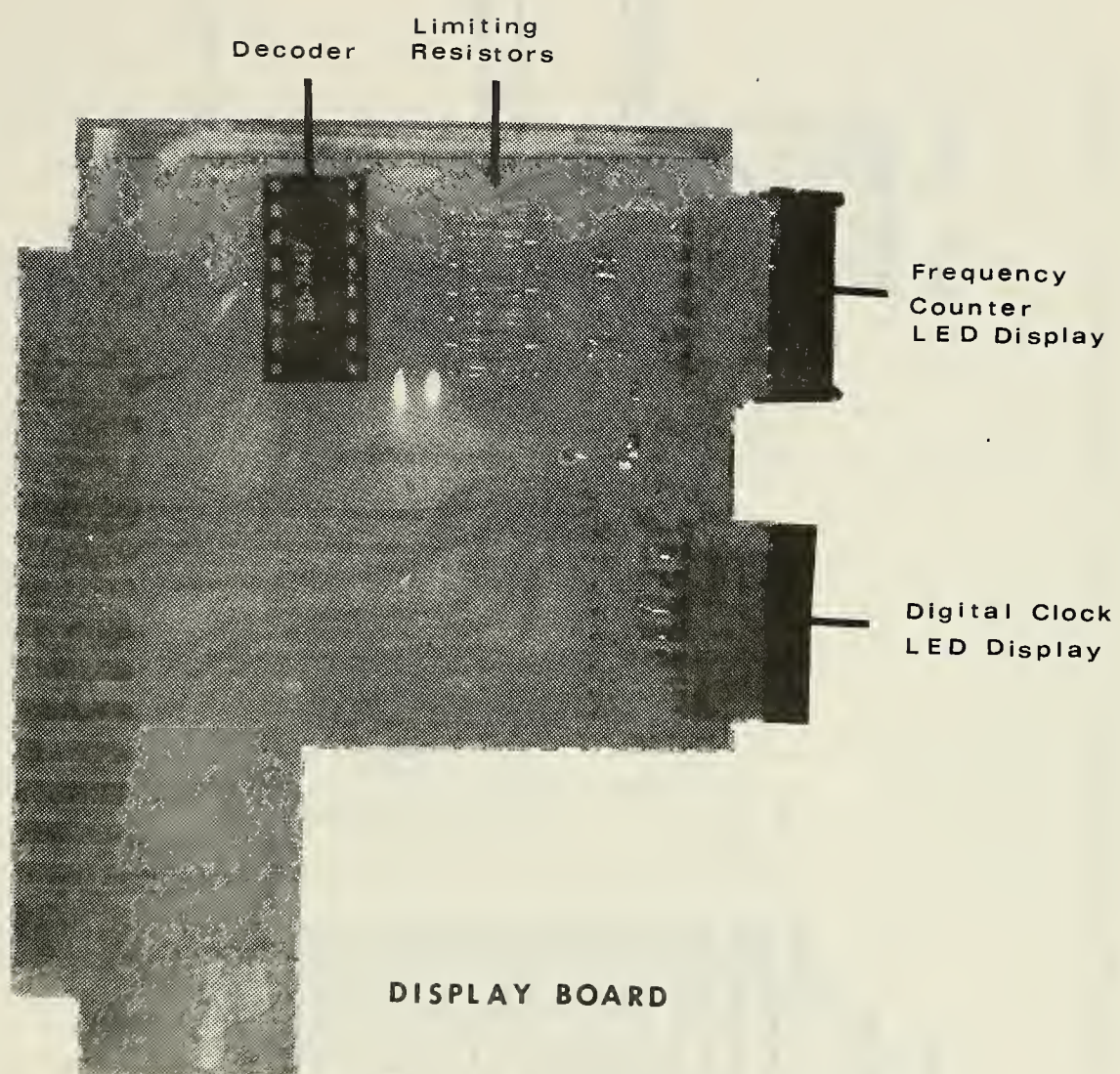


FIGURE 76

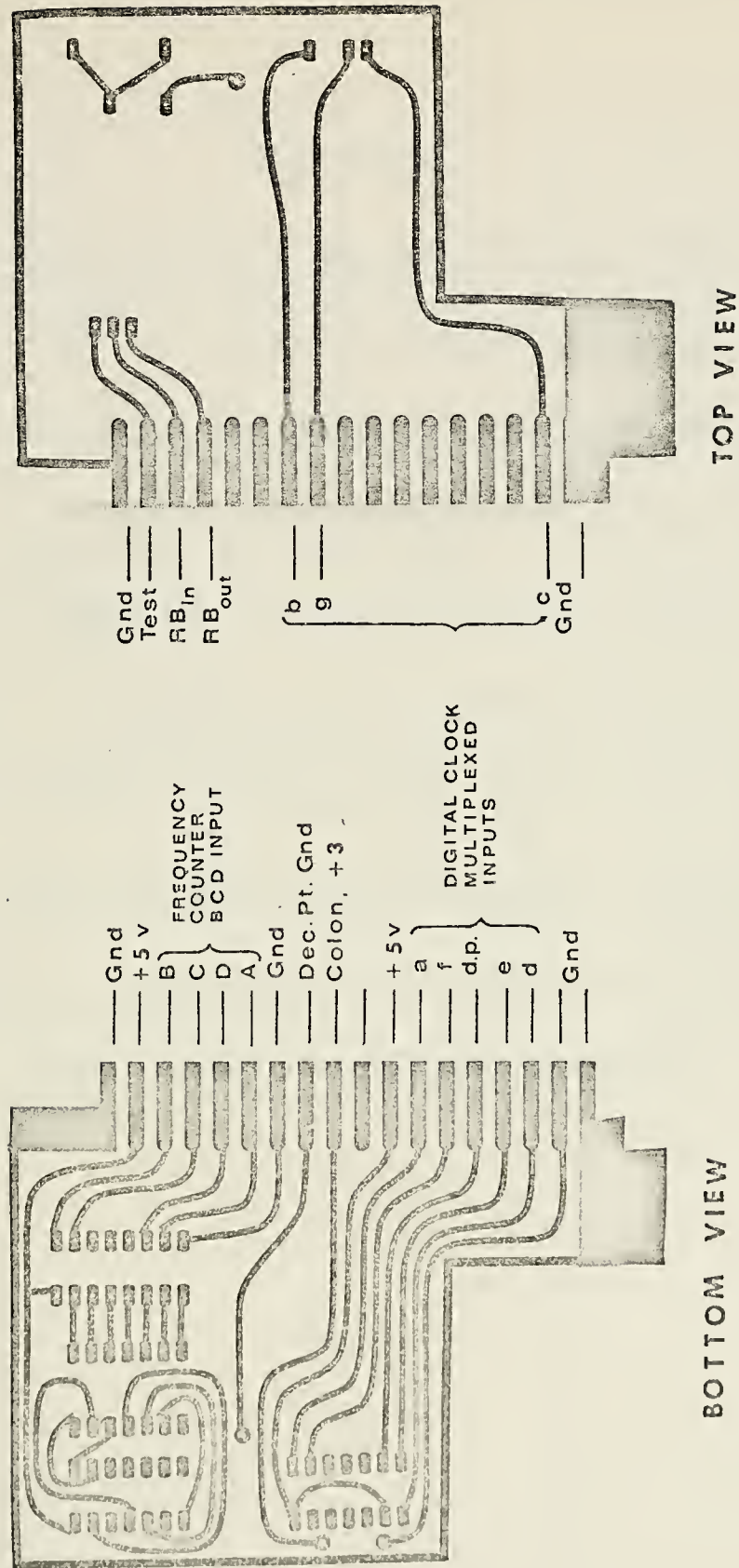


FIGURE 77

BIBLIOGRAPHY

1. Barna, Arped, and Porat, Dan I., Integrated Circuits in Digital Electronics, John Wiley & Sons, 1973.
2. General Radio Corporation, Handbook of Coaxial Microwave Measurements, 1968.
3. Graeme, Jerald G., Applications of Operational Amplifiers, McGraw-Hill, 1973.
4. Hoeschele, David F., Analog-to-Digital/Digital-to-Analog Conversion Techniques, John Wiley & Sons, Inc., 1968.
5. Roman, Stephen, Transmission Lines and Antennas, Holt, Rinehart and Winston, Inc., 1969.
6. Johnson, Walter C., Transmission Lines and Networks, McGraw-Hill, 1950.
7. Kohonen, Teuvo, Digital Circuits and Devices, Prentice-Hall, Inc., 1972.
8. Lenk, John D., Simplified Solid-State Circuit Design, Prentice-Hall, Inc., 1971.
9. Sobel, Herbert S., Introduction to Digital Computer Design, Addison-Wesley Publishing Company, 1970.
10. Toby, Gene E., Graeme, Gerald G., and Huelsman, Lawrence P., Operational Amplifiers, McGraw-Hill, 1971.

DISTRIBUTION LIST

	No. Copies
1. Defense Documentation Center Cameron Station Alexandria, Virginia 22314	2
2. Library, Code 0212 Naval Postgraduate School Monterey, California 93940	2
3. Professor R. Adler, Code 52Ab Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1
4. Professor Jauregui, Code 52 Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1
5. LT. C. Appel, USCG (student) Naval Postgraduate School, SMC-2300 Monterey, California 93940	1
6. Mr. T. Pickering Pickering Radio Company, Inc. Professional Plaza Portsmouth, Rhode Island 02871	1
7. Mr. C. Nelson NELC, Code 2120 San Diego, California 92152	3
8. Mr. Russ Roberts Interstate Electronics Corporation P.O. Box 3117 Anaheim, California 92803	2
9. Mr. T. Green Southwest Research, Inc. P.O. Box 28510 San Antonio, Texas 78284	2
10. Mr. J. Speiser Naval Undersea Center San Diego, California 92132	2
11. Mr. Seth Perry Army Security Agency Arlington Hall Station Arlington, Virginia 22212 IARD-C	1

12.	Mr. J. Griffin NELC San Diego, California 92152	2
13.	LT. Glen Elfers NSG DET Box 99 Naval Sub Base Groton, Conn. 06340	1
14.	LCDR L. Olson CNO OP-009U Pentagon, Washington, D.C.	3
15.	Mr. Wolnowsky Lockheed Missile and Space Co. 1111 Lockheed Way Sunnyvale, California 94088	3
16.	CDR H. Orejuela NAVSECGRU COMM 3801 Nebraska Avenue Washington, D.C. 20390	1
17.	CAPT. W. Hipple ARPA 1400 Wilson Blvd. Arlington, Virginia 22209	1
18.	CDR. R. McCalla NSG Activity Skaggs Island Sonoma, California 94592	1
19.	CDR. J. Pope Office ASDI Pentagon, Washington, D.C.	1
20.	Mr. P. Parsons NSA Ft. Meade, Md. 20755	1
21.	LCDR. Shields NAVELEX PME-107 Washington, D.C.	1
22.	COMNAVSHIPYD MARE ISLAND Atten: LT. D. Patrick Mare Island Naval Shipyard Vallejo, California 94592	3

- | | | |
|-----|--|---|
| 23. | Mr. E. S. Duncan
N. L. & A. I.
1605 N. Elm
Visalia, California 93277 | 1 |
| 24. | Mr. J. Dunlavy
Antenna Research Associates
1101 Clarion Drive
Corpus Christi, Texas 78412 | 2 |

9483187

S-9364

153417

Thesis

P2595

Patrick

c.1

Digital display of
characteristic param-
eters of active radio
frequency transmission
systems.

9483187

S-9364

Thes

P2595

c.1

153417

Thesis

P2595

Patrick

c.1

Digital display of
characteristic param-
eters of active radio
frequency transmission
systems.

thesP2595

Digital display of characteristic parame



3 2768 001 00261 1

DUDLEY KNOX LIBRARY